An Optical Readout System for the LHCb Silicon Tracker

Dissertation

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If there are two or more ways to do something, and one of those ways can result in a catastrophe, then someone will do it.

Capt. Edward A. Murphy, Jr.

Abstract

The LHCb experiment is dedicated to precisely measure the CP-violation parameters in the B-meson decay. It is one of the four large experiments which is currently being installed at the Large Hadron Collider (LHC) and planned to start taking data in 2007. The Silicon Tracker covers the tracking volume around the beam pipe with the highest track densities. The huge amount of data generated during operation has to be transported to the processor farm for follow-up track recognition and analysis.

This work presents a digital optical readout link which transmits the tracking information with a rate of 2.7 Terabit/s over a distance of 100 m from the detector to the computer farms. Special attention was paid to the radiation tolerance of the transmitting section, as its location is exposed to ionizing particles and radiation levels similar to those encountered in space applications. The design was aimed to provide a modular system which simplifies production, testing, commissioning and maintenance. Where possible, commercial off-the-shelf components were used to reduce the overall cost of the system. For commercial components exposed to radiation, several irradiation campaigns were performed to qualify them for use in the LHCb environment.

Zusammenfassung

Das LHCb Experiment ist auf die präzise Messung von Parametern ausgelegt, welche die Verletzung der CP-Symmetrie im Zerfall von B-Mesonen beschreiben. Es ist eines der vier grossen Experimente, welche zur Zeit am Large Hadron Collider (LHC) installiert werden und 2007 mit der Datennahme beginnen sollen. Der Silizium Spurdetektor deckt hierbei die Bereiche mit den höchsten Spurdichten ab. Die enorme Datenmenge, welche während der Datennahme erzeugt wird, muss zu der Prozessorfarm transportiert werden, welche die nachfolgende Spurerkennung und Analyse durchführt.

Diese Arbeit stellt ein digitales optische Auslesesystem vor, welche die Spurinformationen mit einer Datenrate von über 2.7 Terabit/s über eine Entfernung von 100 m zu der Computerfarm übertragt. Besondere Aufmerksamkeit wurde der Toleranz des sendenden Teils gegenüber ionisierender Strahlung gewidmet, da dieser direkt am Detektor sitzt und somit Strahlungsdosen ausgesetzt ist, welche vergleichbar zu denen in Raumfahrtanwendungen sind. Der Entwurf zielte darauf ab ein modulares System bereitzustellen, welches die Produktion, das Testen, die Inbetriebnahme und die Wartung vereinfachen soll. Kommerzielle Bauteile wurden so oft wie möglich verwendet, um die Gesamtkosten des Systems zu reduzieren. Komponenten, welche ionisierender Strahlung ausgesetzt werden, wurden verschiedenen Bestrahlungstests unterzogen, um sie für den Einsatz unter LHCb Bedingungen zu qualifizieren.

Contents

Introduction

Astronomical observations suggest, that our universe developed from an infinitely dense and energetic state after the 'big bang'. One of the most intriguing questions for particle physicists is the absence of antimatter, the counterpart of ordinary matter, in the observable universe. This is concluded from the lack of observed annihilation between matter and antimatter, which would occur in space regions, where both exist next to each other. CP violation is one neccessary ingredient to generate such an asymmetry. Although the Standard Model of Particle Physics predicts the violation of CP symmetry, its value is too small to explain the observed imbalance between matter and antimatter. Other sources for CP violation have to exist, which can be determined by measuring the deviation of its parameters from the Standard Model predictions.

Collisions of highly accelerated subatomic particles can generate particles, which are believed having played a key role in developing this asymmetry. The LHCb experiment is dedicated to characterize the CP violation in the system of B-mesons with high precision. It is presently under construction at the LHC particle collider at CERN, which is planned to start taking data in 2007.

A central element of any high energy physics experiment is the tracking system, which records the flight paths of charges particles created in the collisions. Together with a magnetic field, it allows in addition the precise determination of the momentum of a particle. For areas with high track density, silicon strip sensors are used in the LHCb detector.

This thesis presents the digital optical readout, which has been developed for the Silicon Tracker of the LHCb experiment. The primary task for this readout system is to transmit the detector data with a total data rate of just under 3 Terabit/s to the processing computers which are located at a distance of about 100 m from the detector. A design constraint is the required radiation tolerance as the transmitting section is located close to the detector.

This thesis is organized as follows:

Chapter 1 gives a brief introduction into the theoretical background of CP violation, with special focus on B-meson decays. The LHCb experiment is presented in a short overview in Chapter 2.

The Silicon Strip detector as a detection device is discussed in Chapter 3, followed by a description of the LHCb Silicon Tracker in Chapter 4. Chapter 5 presents the Beetle

readout chip, which amplifies the detector signals before transmission. Its performance and the resulting implications for the data digitization are discussed.

In Chapter 6, a general overview of the digital optical readout system is shown with results from sub-system prototyping following in Chapter 7. The radiation qualification of components is documented in Chapter 8.

The interfaces to common LHCb systems are described in Chapter 9. In Chapter 10, the Service Box as a key element of the Silicon Tracker readout chain is characterized. The data is received at the first stage of the common LHCb data acquisition network, which is shown in Chapter 11. Chapter 12 gives an outlook on the effort to unify all optical data networks of the experiment into a common LHCb optical link system.

A summary of the developments concludes this thesis.

Chapter 1

CP Violation in B-meson Decays

The electro-weak sector of the Standard Model of particle physics has been tested and verified with a large number of experiments and to a high level of precision. Still, the Standard Model is known to be incomplete. Important aspects remain unexplained, like the origin of the masses of particles or the values of fundamental parameters. Many efforts are undertaken to determine the exact nature and size of these effects. One promising approach to further test the Standard Model are measurements in the b-quark sector, which can be carried out by studying decays of B-mesons. In particular, new physics beyond the standard model can be probed by precisely determining the size of CP violation in the B-meson system, .

CP is the combined transformation of the charge conjugation C and the parity transformation P. While parity transformation is a simple inversion of all space coordinates, charge conjugation converts a particle into its antiparticle. In 1957, it was shown in the beta decay of polarised Co-60 atoms, that parity symmetry is maximally violated in weak interactions [1]. By investigating the decay of muons, which is also mediated by the weak force, it became clear that charge symmetry was also maximally violated, so that the combined symmetry of CP could be conserved. However, CP violation was experimentally discovered in 1964 in the decay of K-mesons [2], by observation of the CP-forbidden two-body decay $K_L \to \pi^+\pi^-$.

CP Violation in the Standard Model

CP violation can be described in the Standard Model via a complex phase in the Cabbibo-Kobayashi-Maskawa (CKM) matrix, which describes the mixing of the flavour eigenstates of the quarks into their mass eigenstates.

$$V_{CKM} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix}$$

The nine complex matrix elements are not independent from each other and can be reduced to a set of four parameters, three real rotation angles and one complex phase. In the Wolfenstein parametrisation [3], the parameters A, λ, ρ, η are used, where $i\eta$ describes the complex phase. Expanding in orders of $\lambda = |V_{us}| \approx 0.22$, the CKM matrix can be written as:

$$V_{CKM} = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3(\rho - i\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1 - \rho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4)$$

CP violation occurs for a non-zero value of the parameter η. From the size of λ, it is clear that the diagonal elements of V_{CKM} are close to 1 while the off-diagonal elements are small. The assumption of three quark families leads to the unitarity constraint:

$$V_{CKM}^{\dagger} V_{CKM} = V_{CKM} V_{CKM}^{\dagger} = 1$$

This leads to nine equations, six of which have a result of zero and can be plotted as triangles in the complex plane. Two of these triangles are especially interesting, as the length of their sides are all of the same order $\mathcal{O}(\lambda^3)$. The corresponding equations are:

$$V_{ud} V_{ub}^{*} + V_{cd} V_{cb}^{*} + V_{td} V_{tb}^{*} = 0$$

$$V_{tb} V_{ub}^{*} + V_{ts} V_{us}^{*} + V_{td} V_{ud}^{*} = 0$$

The base of the triangles is usually normalized by dividing by the second term of the first equation, $V_{cd} V_{cb}^{*}$. Up to $\mathcal{O}(\lambda^3)$, the two triangles coincide. With the increased precision of the LHC experiments, higher orders of λ have to be taken into account, resulting in these two triangles (Figures 1.1, 1.2) being separated.

B-meson Decays

B-mesons are quark-antiquark pairs of one b-antiquark and a (u,d,s,c)-quark. The study of B-meson decays is a key process for the precise determination of the CP violating parameters. Large asymmetries are predicted and can be calculated with small theoretical uncertainties. Furthermore, measurements are possible in many different decay channels, permitting to overconstrain the unitarity triangles.

The quantities V_{cb} and V_{ub} can be determined from the various B-meson decays generated by tree diagrams. Furthermore, V_{td} and V_{ts} can be calculated from the $B_d^0\overline{B_d^0}$ and $B_s^0\overline{B_s^0}$ oscillation frequencies, assuming that oscillations proceed only via the known Standard Model

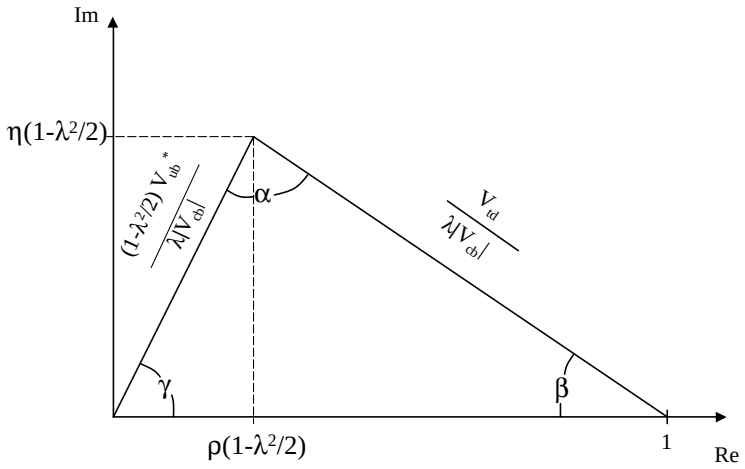

Figure 1.1: Graphical representation of the first unitarity triangle approximated up to $\mathcal{O}(\lambda^5)$.

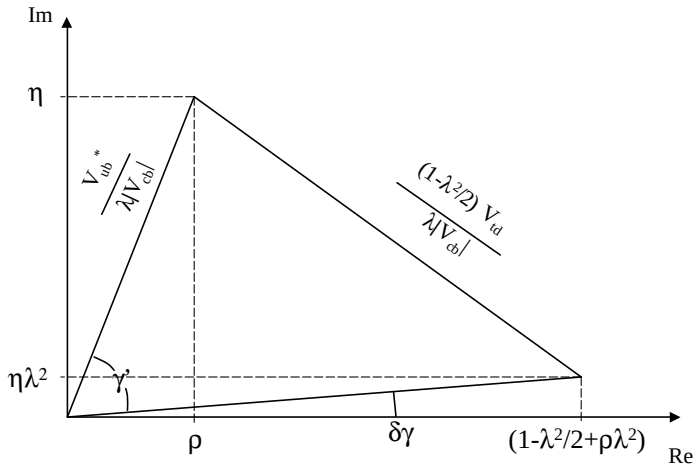

Figure 1.2: Graphical representation of the second unitarity triangle approximated up to $\mathcal{O}(\lambda^5)$.

box diagrams. Currently, the $B_d^0\overline{B_d^0}$ oscillation frequency is very well measured, but only a lower limit is known for the $B_s^0\overline{B_s^0}$ oscillation frequency. Combined, these measurements determine two sides of the triangle shown in Figure 1.1 and thus permit to construct the triangle and extract the parameters A, ρ and η.

Since 1999, two dedicated experiments have been investigating the decays of B-mesons originating from the decay of the $\Upsilon(4S)$-resonance. BaBar at SLAC and BELLE at KEK-B have both seen evidence for a large CP violation in the B-meson system and measured a value

of 0.724 ± 0.049 for the value of $\sin 2\beta$, in excellent agreement with theoretical predictions [4][5].

As a result, the Standard-Model CKM mechanism as outlined in the previous section is considered to be a good theory to explain the CP effects in flavour changing processes both in the Kaon and the B-meson systems. Therefore this field can be used to perform precision measurements to search for possible small corrections to the theory due to unknown new physics.

Recently, the BaBar and BELLE collaborations have presented first results on the observation of so-called "direct" CP violation in the decay of neutral B-mesons. In contrast to the B-$\overline{\mathrm{B}}$ oscillation, in which CP violation manifests itself in a time dependent decay rate asymmetry of B and $\overline{\mathrm{B}}$ into the same final state, which is a CP eigenstate, here the decay rates of B and $\overline{\mathrm{B}}$ into CP conjugated flavour specific final states are compared. In particular, the decays $\mathrm{B}^0_\mathrm{d} \to \mathrm{K}^+\pi^-$ and $\overline{\mathrm{B}^0_\mathrm{d}} \to \mathrm{K}^-\pi^+$ were studied and their branching ratios were found to be different. The combined result from Belle and BaBar yields a relative rate asymmetry of $\mathrm{A_{CP}} = -0.114 \pm 0.020$, which is consistent with the Standard Model prediction of large direct CP asymmetries in the B-meson sector.

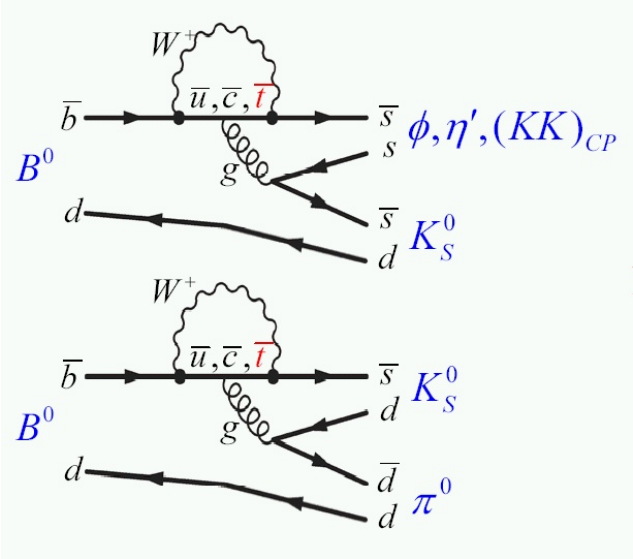

Figure 1.3: The Standard Model penguin diagrams for the decay processes $\mathrm{b} \to \mathrm{s\bar{s}s}$ and $\mathrm{b} \to \mathrm{s\bar{d}d}$.

Furthermore, the BaBar and Belle collaborations have recently presented preliminary results on the measurement of CP asymmetries in the decay $\mathrm{B}^0_\mathrm{d} \to \phi \mathrm{K_S}$ and other decays of the type $\mathrm{b} \to \mathrm{s\bar{s}s}$ and $\mathrm{b} \to \mathrm{s\bar{d}d}$. In the Standard Model, these decays proceed through penguin diagrams such as illustrated in Figure 1.3. The experimental errors for individual decay channels are still large, but the averages for the CP-asymmetry for each of the two experiments, namely [6]

$$\sin 2\beta' = \begin{cases} 0.42 \pm 0.10 & \text{BaBar} \\ 0.43 \pm 0.12 & \text{Belle}\,, \end{cases}$$

are in good agreement with each other. However, the Standard Model predicts $\beta = \beta'$ and thus there is a discrepancy of 2.7 respectively 2.4 standard deviations. This is the largest but one experimental discrepancy [7] from Standard Model predictions presently known.

However, due to the mass of 10.58 GeV of the initial $\Upsilon(4S)$ state, only $B^{\pm}$ and $B^0_d/\overline{B^0_d}$ can be investigated in these experiments. With the much higher center-of-mass energy available at the LHC, $B^0_s/\overline{B^0_s}$ mesons become available in addition, allowing a much wider range of measurements that will permit to overconstrain the unitarity triangles. Due to a large number of B-mesons produced at the LHC, the study of rare B-decays provides another means to search for new physics beyond the Standard Model.

Chapter 2

LHC and the LHCb Experiment

The LHC accelerator is a proton-proton collider with a center-of-mass energy of 14 TeV (see Figure 2.1). Although the luminosity will be up to 10^{34} cm^{-2}s^{-1} for the experiments ATLAS and CMS, LHCb will run at a lower luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} to maximize the number of events with single p-p interactions. Multiple interactions in one event would lead to more than one primary vertex, which would make the determination of secondary vertices impossible. A clear indentification of secondary vertices is mandatory for fast triggering on events containing B-mesons. The bunch crossing frequency of about 25 ns requires fast electronics to provide deadtime-free readout of the detectors. The high interaction rate combined with elevated particle multiplicities in the forward direction lead to a high radiation load on the detectors and the on-detector electronics.

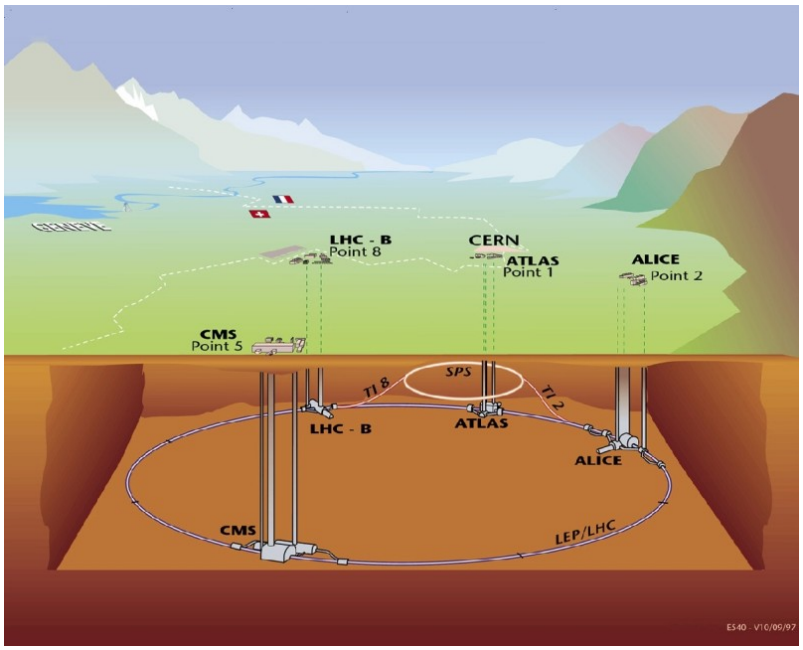

Figure 2.1: The LHC accelerator at CERN.

LHCb has been optimized to record decays of B-mesons produced in p-p collisions. The LHCb detector (Figure 2.2) makes use of the forward peaked production cross section of the B-mesons by covering only a small angular region around the beampipe. The detector consists of a single arm spectrometer with a warm 4 Tm dipole magnet. The experiment is set up in the former DELPHI pit at Intersection Point 8 of the LEP/LHC tunnel. The nominal p-p interaction point was displaced by 11.25 m, just into the LHC tunnel. By doing so, the full volume of the pit was made available for setting up the LHCb detector.

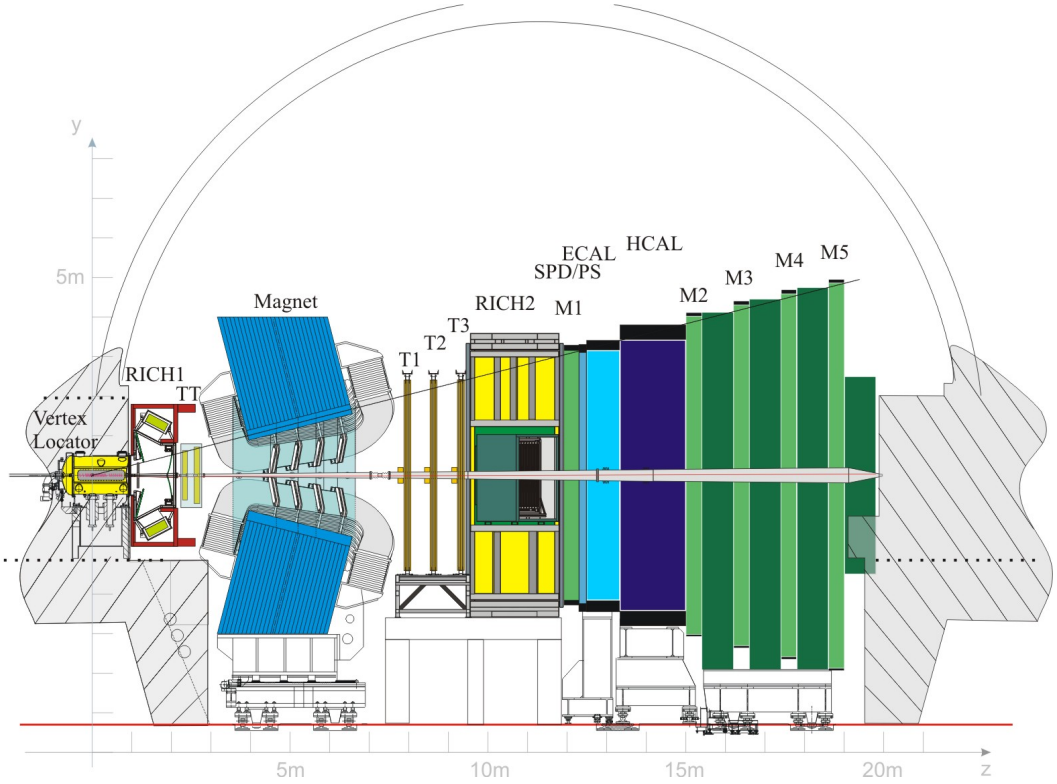

Figure 2.2: The LHCb detector.

Located directly around the p-p interaction point, the Vertex Locator (VELO) provides precise position information to determine secondary vertices generated by decaying B-mesons. This is important for time-dependent measurements of CP-asymmetries and a precise measurement of the $B_s^0 - \overline{B_s^0}$ oscillation length. The tracking system covers 250 mrad in the non-bending plane and 300 mrad in the bending plane of the spectrometer magnet. It consists of one tracking station in front of the magnet (Trigger Tracker or TT) and three tracking stations (T1-T3) behind the magnet. While the Trigger Tracker is realized completely with silicon detectors, the stations T1-T3 have silicon detector coverage only close to the beam pipe, where the track density is highest. This system is called the Inner Tracker (IT). Farther out, straw tube detectors of the Outer Tracker (OT) with coarser granularity are used to cover the remaining area of the acceptance angle. For hadron identification, two Ring Imaging Cherenkov counters (RICH-1 and RICH-2) are placed upstream and downstream of the tracking system. Following the RICH-2 detector are the calorimeter system consisting of a preshower detector, an electromagnetic and a hadronic calorimeter (PS, ECAL, HCAL), and

the Muon detector (M1-M5).

The production cross section of B-mesons is only about 1 % of the visible cross section. In addition, the expected branching ratios for most of the interesting decay channels are in the order of 10^{-5}, which leads to a high ratio of background events to signal events. The LHCb experiment needs therefore an efficient yet robust and flexible trigger system (Figure 2.3) to select the events containing decays to be studied. The LHCb design luminosity of $2 \cdot 10^{32}$ cm^{-2}s^{-1} translates into an average p-p interaction rate of about 10 MHz. Making use of the high B meson mass and the resulting high transverse momentum of the decay products, the Level-0 trigger uses tracks with high transverse momentum in the muon system and clusters with high transverse energy in the calorimeter to generate a L0-accept decision within 4 μs. Data from a Pile-Up detector is included in the L0 decision to veto events with multiple p-p interactions. The average Level-0 trigger rate is 1 MHz and this is the input rate for the Level-1 trigger algorithm.

The decay products of the B-mesons originate from a displaced secondary vertex due to the long lifetime of the B-mesons. The Level-1 trigger uses data from the Vertex Locator and the Trigger Tracker to look for tracks with both high transverse momentum and large impact parameter with respect to the primary p-p interaction vertex. The Level-1 accept rate is about 40 kHz.

A pipelined architecture is used to temporarily store data on Level-0 and Level-1 buffers, while the according algorithm decides whether to keep an event or reject it. If a trigger accept is received, the pipeline control logic can extract the triggered event as the trigger latency is fixed and known. This enables to run the complete experiment without any readout induced deadtime. The length of the pipelines is equal to the maximum input rate multiplied by the maximum execution time of the trigger algorithm. For the Level-0 pipeline, which is directly implemented in the frontend readout chips, this leads to a pipeline length of 160 events, as specified in [9]. Upon a Level-0 accept, the data is sent to the Level-1 preprocessors, where the data is stored in a second pipeline during execution of the Level-1 trigger algorithm. The Level-1 preprocessor boards are not located on the detector anymore due to their increased complexity, but in the counting house, which is located in a radiation shielded area, about 100 m away from the detector. It is therefore required to transmit the detector information at a trigger rate of about 1 MHz from the frontend readout electronics on the detector to the off-detector Level-1 electronics. The Level-1 buffer of over 58000 events allows for a maximum Level-1 algorithm execution time of 52 ms. The events accepted at Level-1 are sent to the following Higher Level Trigger (HLT), which uses the complete detector information for a final decision on which events are written to the storage tapes.

For the offline reconstruction of an event, the full topology of the decay and its decay products have to be recorded. This includes measuring the energy of the particles, identifying the particles and determination of their momentum. For the latter, the deflection of their trajectory when passing the magnetic field of the dipole magnet is needed. As a result, a precise track determination is necessary to provide the required momentum resolution for high-quality studies of the B-meson decay.

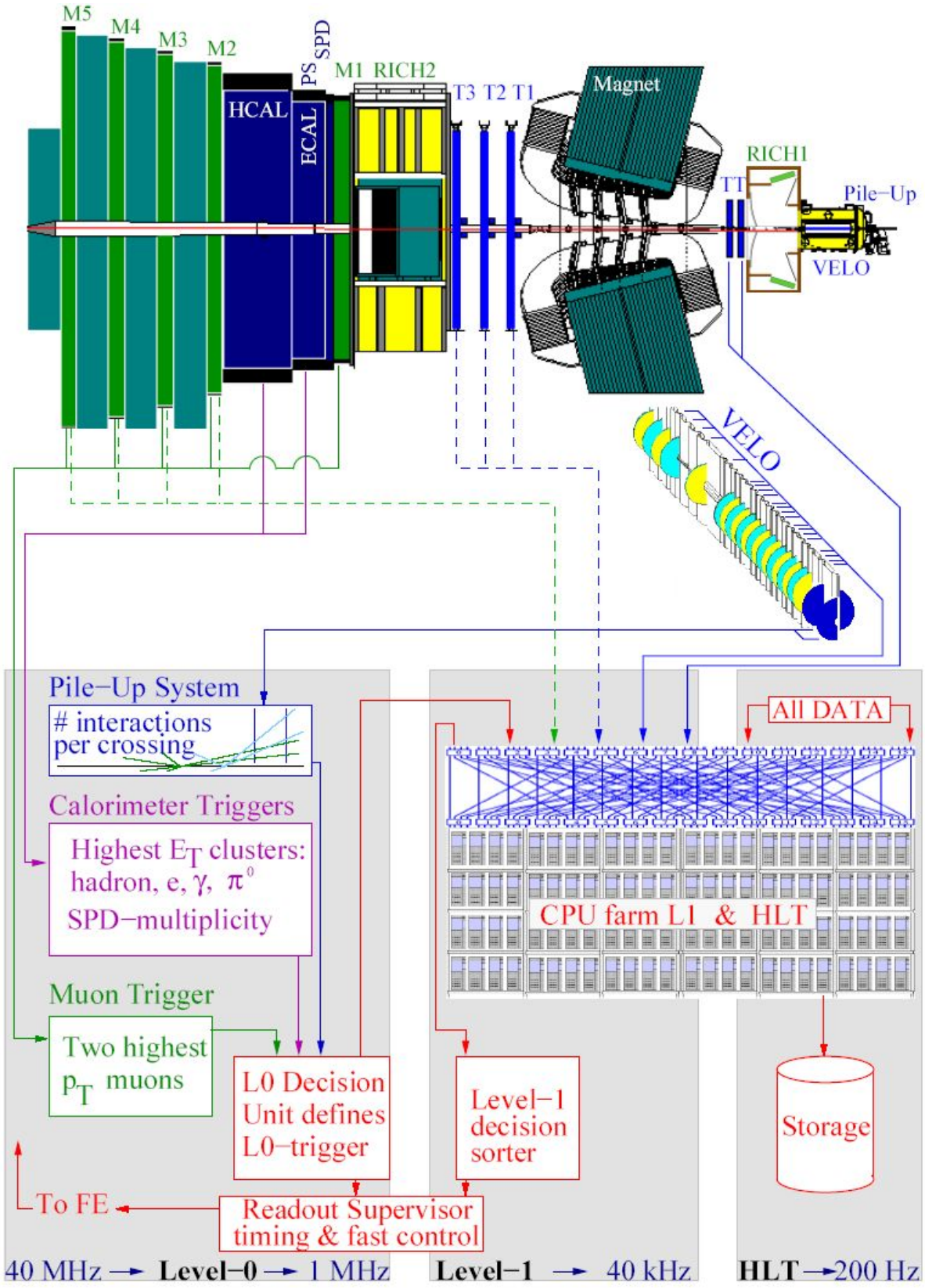

Figure 2.3: General triggering scheme of LHCb[8].

Chapter 3

Silicon Strip Detectors

The detection of charged particles in the LHCb Silicon Tracker is based on single-sided silicon micro-strip detectors. This chapter presents the principle of particle detection by silicon detectors, discussing both signal and noise generation. As the detectors will be subjected to high radiation levels in the LHCb environment, the effects of radiation on the detector's performance is also briefly outlined.

3.1 Signal and Noise Generation in Silicon Detectors

A diode is one of the simplest semiconductor devices. It features two differently doped semiconductor materials and the contact region in between them, the pn-junction. The free charge carriers of the n-doped material have negative sign (electrons) while the p-doped material features positively charged holes, which contribute to the electric current. At the junction, the free charge carriers from both doped regions recombine. Therefore, this junction is lacking free charge carriers and is called depletion zone. As the charge carriers which are fixed to the crystal lattice cannot recombine, they generate an electric field in the depletion zone. Any additional charge carriers, which are for example generated by ionizing particles traversing the depletion zone, are accelerated in the electric field and generate an electric current. For a more detailed discussion on semiconductor physics see also [10].

While theoretically any partially depleted pn-junction detects ionizing radiation and particles, the detection efficiency is rather limited due the small thickness of the depleted zone. By applying a reverse voltage, the depleted thickness can be increased to the wafer thickness and the detection capabilities are greatly enhanced. To further obtain information about the position of the particle passage through the detector, one side the pn-junction has to be segmented and read out individually per channel. One of the basic forms of segmentation in one dimension leads to the single-sided silicon strip detector, as illustrated in Figure 3.1.

The detector has a fully metallized backplane for connection of the bias voltage. As bulk material, n-doped semiconductor material is typically used due to its widespread use in the

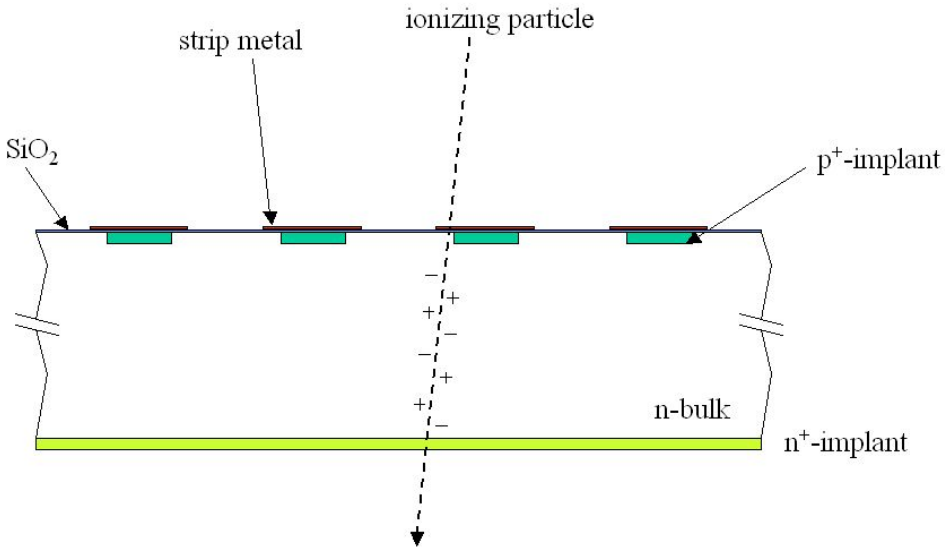

Figure 3.1: cross section of a silicon strip detector.

semiconductor industry. The strip geometry is realized with p-doped implants on the upper side. The pn-junction is formed between the bulk and the segmented implants. While the p-implants could in principle be directly connected to a readout amplifier, an AC-coupling is preferred in our case to prevent high leakage current to pass through and saturate the amplifier. To achieve the AC-coupling, a metal strip is located just above the strip implants, with a thin layer of isolating SiO_2 in between. The naturally forming depletion zone of the pn-junction is enlarged to the full detector thickness by applying a reverse bias voltage. When the bulk is made from n-doped silicon and the implants are p-doped, the reverse bias is applied by grounding the p-implants and connecting the backplane of the n-bulk to positive voltage.

3.1.1 Signal

The most probable energy loss of a minimum ionizing particle (MIP) penetrating the depleted silicon is about 270 eV/μm according to the Bethe-Bloch equation for energy loss of ionizing particles [11]. As the mean energy needed for the creation of an electron-hole pair is 3.62 eV, this results in a most probable value of the number of electron-hole pairs of approximately 23800 for 320 μm thick silicon, 30500 for 410 μm thick silicon and 37300 for 500 μm thickness. The electrons and holes are separated in the electric field inside the depletion zone and drift to the backside of the sensor and to the strip implants, respectively. The drift velocity of charge carriers in matter can be calculated as:

$$v_{drift} = \mu \cdot E$$

where E is the electric field and μ is the mobility of the charge carrier, which is also dependent on E. For typical field strengths of 0.5 V/μm in the silicon sensor, the mobilities

are given in Table 3.1. In addition, typical drift times for a drift length of 500 μm are given.

Table 3.1: Mobility of charge carriers and typical drift times for a drift length of 500 μm and an electric field of 0.5 V/μm (taken from [12]).

charge carrier	mobility [10^6 cm^2/(V $\cdot$ s)]	drift time [ns]
electrons	7.0	7.1 ns
holes	2.5	20.0 ns

The charge carriers drift along the electric field lines and induce an electric current into the strip implants closest to their location. The size of the induced current from a single moving charge carrier is depending on its drift velocity and its current distance to the corresponding implant (see also [12]).

3.1.2 Noise

Contrary to gaseous detectors or avalanche photodiodes, no charge multiplication takes place in a silicon strip detector. Therefore, low-noise frontend amplifiers are needed for efficient signal detection. One has to distinguish between two types of noise according to their source.

Thermal or Johnson noise The thermal noise power of a resistor is generated by thermal agitation of electrons in a conductor. It is intrinsic to any resistor and is proportional to the recorded bandwidth B and to the temperature T of the resistor, but not to its value.

$$P_{thermal} = 4 \cdot k \cdot T \cdot B$$

The spectral density of this noise is constant ('white noise'). When applying this formula to a silicon strip detector, the interesting quantity is the noise in electrons, measured by the charge integration preamplifier. Therefore, the noise power is typically converted into a equivalent noise charge (ENC):

$$U^2_{thermal} = P \cdot R$$
$$ENC_{thermal} = C_{strip} \cdot U_{thermal}$$
$$ENC_{thermal} = C_{strip} \cdot \sqrt{4 \cdot k \cdot T \cdot B \cdot R}$$

The thermal ENC therefore linearly depends on the equivalent capacitance C_{strip} at the input of the charge preamplifier. It also depends on the bandwidth of the readout chain, with a smaller bandwidth leading to a decreased noise.

Shot noise Despite being reversely biased, any silicon strip detector will exhibit leakage current as described in Section 3.1, which is generating shot noise. The origin of the shot noise is the random motion of the electrons as they are discrete charge carriers. Its magnitude is expressed as the variance of the current and is proportional to the current itself. It has a white spectral distribution, like the thermal noise.

$$i^2 =< (I- < I >)^2 >= 2 \cdot e \cdot I_{leak} \cdot B$$

Therefore, a small leakage current is necessary for low-noise operation of any silicon sensor.

Chapter 4

The LHCb Silicon Tracker

The main purpose of the LHCb tracking system is to record precisely the tracks of charged particles in the detector. The particle's momentum and its sign of charge can be determined by measuring the deflection of its trajectory when passing the magnetic dipole field. The accuracy of the track measurement determines the momentum resolution, hence good spatial resolution of a precisely aligned tracking detector is needed. In addition, any multiple scattering at the material of the detector itself has to be minimized for precisely measuring low momentum particles. The Silicon Tracker was therefore designed with a low material budget inside the acceptance of the detector. The channel occupancy of the detector has to be kept low to simplify the track reconstruction. This requires a fine granularity, regardless of the needed spatial resolution. Due to the high track density around the beampipe and close to the interaction point, silicon strip detectors were chosen for the Trigger Tacker, which is located in front of the magnet, and the innermost region of the tracking stations T1-T3, which are referred to as the Inner Tracker.

4.1 Trigger Tracker

The Trigger Tracker is an all-silicon station which covers the full LHCb acceptance at a z-position of 2.47 m just in front of the magnet. The coordinate system of the LHCb detector is shown in Figure 2.2. Figure 4.1 shows a front view of the TT station. The overall dimension of the active area is approximately 160 cm in width and 135 cm in height. It is subdivided in two half-stations (TTa and TTb), which are separated in z-direction by about 30 cm. Each of the two half stations consists of two detection layers built of silicon strip detector modules. The general orientation of the strips is vertical with one layer of each half station having the strips oriented exactly vertical and the second layer rotated by 5 degrees around the z-axis. The spatial resolution in the bending plane of the dipole field is well below 70 μm for a single measurement. While a finer strip pitch would improve the single hit resolution, the momentum resolution would improve only marginally [13]. The relatively large pitch of 183 μm minimizes the number of readout channels for the given area and hence reduces the overall cost for the detector readout.

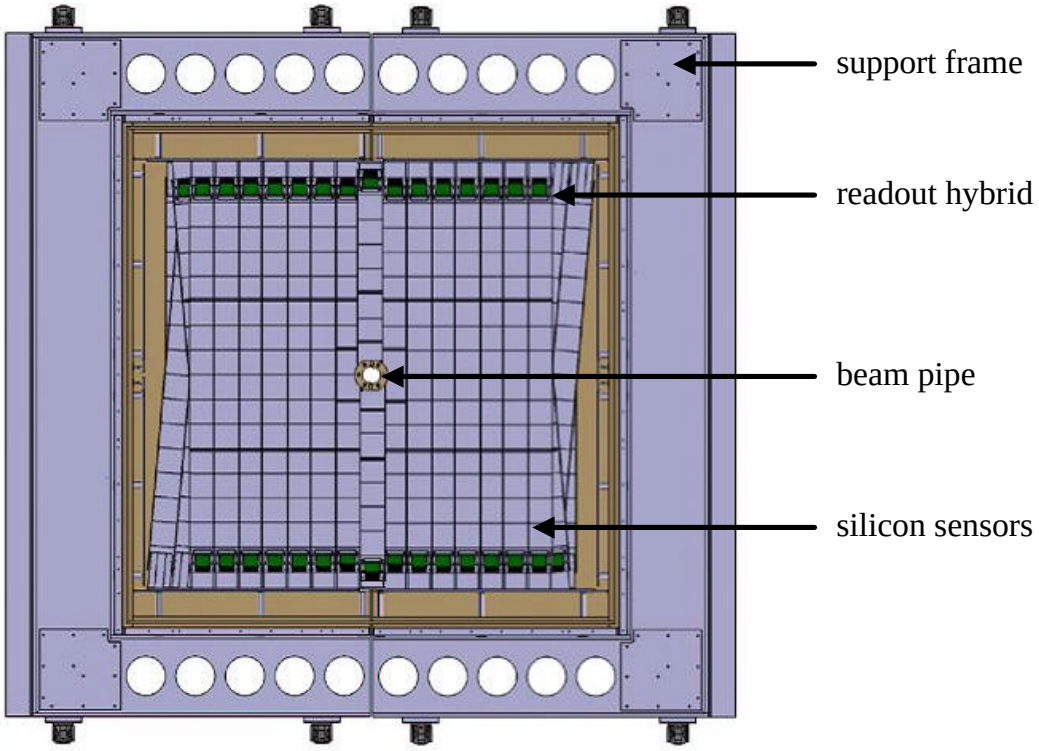

Figure 4.1: Front view of the TT-station.

Long readout strips covering the full height of the TT station would lead to unacceptably large strip capacitances. Building each silicon detector module from several readout sectors reduces the strip capacitance per readout channel. To limit in addition the hit occupancy on the strips, each detection layer of the TT-station was partitioned as shown in Figure 4.2. While the readout sectors at the upper and lower end of each module are made of four silicon strip sensors, the inner sectors consist of three sensors connected in series. For the area directly around the beampipe, a three-sensor readout sector is further divided into a one-sensor and a two-sensor readout sector. Each silicon sensor has 512 strips and a size of 94 x 96 mm^2.

The readout electronics are located on both module ends to minimize the amount of material inside the detectors's acceptance. While the outer 4-sensor readout sectors can be connected directly to the readout hybrids, polyimide cables are used to connect the strips of the inner sectors to the readout electronics. The total load capacitance at the input of a readout amplifier depends on the number of sensors and the length of the connected cable. Measured values for the different TT-sectors are given in Table 4.1. The capacitances include 3 pF to account for bond wires and the pitch adapter from the sensors to the readout hybrid. To obtain a sufficiently high signal-to-noise ratio, the thickness of the TT silicon detectors

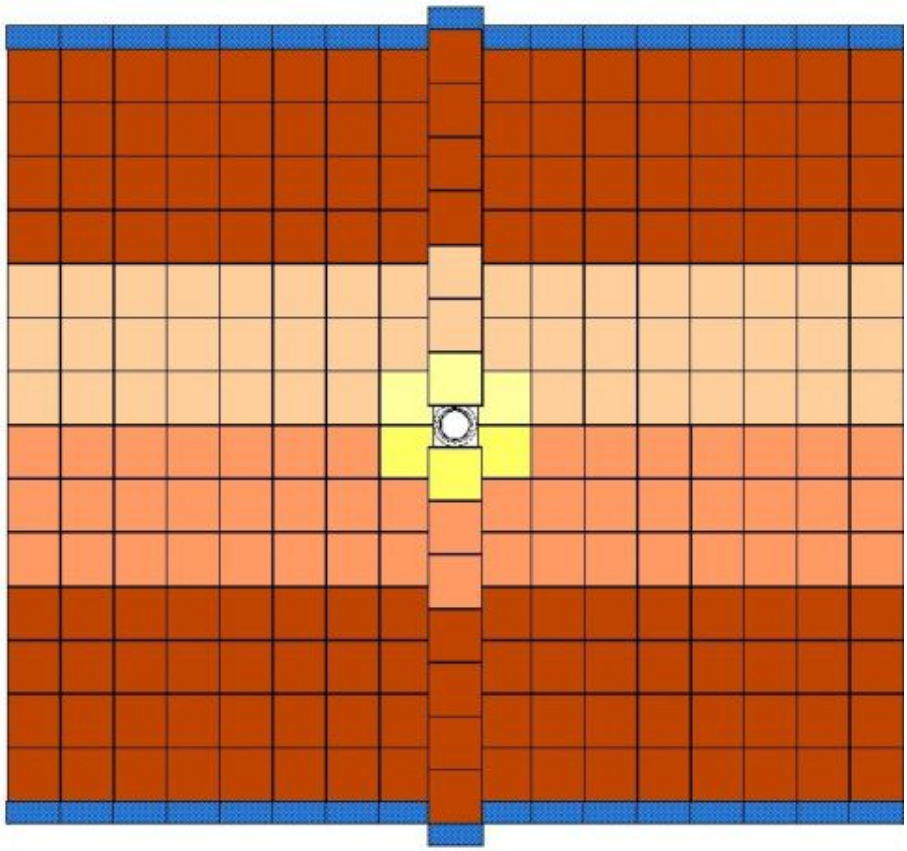

Figure 4.2: Partitioning into readout sectors for one layer of the TTb half-station.

was chosen to be 500 μm.

Table 4.1: Total strip capacitance for different readout sectors of the TT-station (from [14]).

number of sensors	sensor length [cm]	polyimide cable length [cm]	total strip capacitance [pF]
1	9.44	58.0	41.4
2	18.88	39.1	47.1
3	28.32	39.1	60.3
4	37.76	-	57.9

For production reasons, each sensor ladder is built from two half-modules. Each half-module is constructed from seven silicon sensors and a baseplate, which holds the readout hybrids. The silicon sensors are mechanically joined to each other and to the baseplate with carbon fibre support rails, which are glued along the sensor edges. To match the thermal expansion coefficient of the baseplate to the sensors, aluminum nitride was used as baseplate material. The readout hybrid for the 4-sensor section is directly glued on the baseplate. The hybrid for the inner readout sector, which connects to the polyimide cables, is stacked on top of the first hybrid with a copper support for good thermal conductivity to the baseplate. For

a half-module featuring a two-sensor and a one-sensor sector, two hybrids are stacked above the hybrid on the baseplate. The baseplate of each module is mounted on a cooling plate, that is integrated into the frames of the TT-station. This cooling plate also provides the reference for the accurate positioning of the ladders. A sketch of an assembled half-module is shown in Figure 4.3.

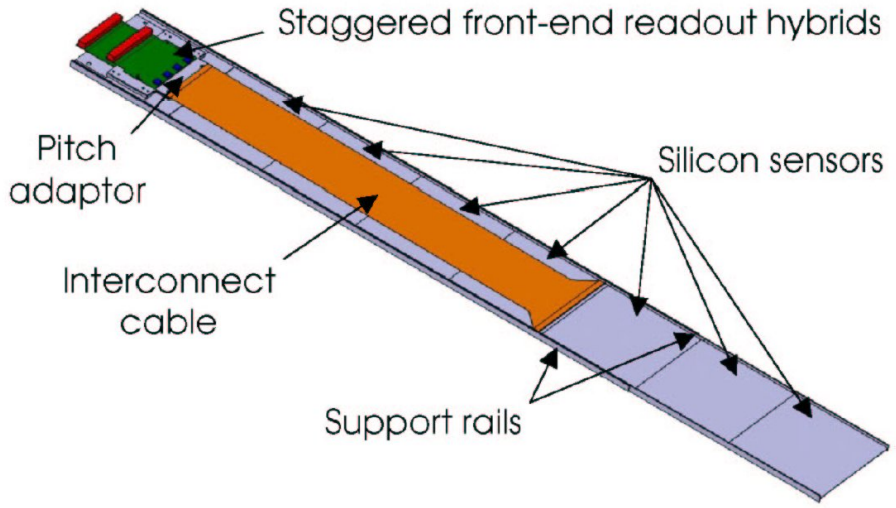

Figure 4.3: View of a half-module for the TT station.

The active silicon area of the complete Trigger Tracker has a size of 7.7 m^2 with 280 readout sectors of 512 strips each. This results in a total number of 143360 readout channels sampled once every 25 ns.

4.2 Inner Tracker

The Inner Tracker (IT) is part of the tracking stations T1-T3 located downstream of the magnet. The Inner Tracker is built from silicon strip detectors and covers the central region around the beampipe where track densities are highest (Figure 4.4). Figure 4.5 shows a detailed view of the Inner Tracker station T2. The layout and dimensions are chosen to keep the occupancy in the Outer Tracker at an acceptable level.

Each Inner Tracker station is split into four independent detector boxes. The upper and lower boxes are equipped with seven one-sensor modules per detection layer, the modules located in the bending plane are housing seven modules per layer with two sensors each connected in series. The IT sensors have a strip pitch of 198 μm and a size of 78 x 110 mm^2. This leads to a number of 384 strips per sensor. Every detector box includes four detection layers, with the same stereo angle arrangement (0, +5, -5, 0 deg) as the Trigger Tracker. The IT detector boxes therefore house 28 sensor modules each. The mechanical support for the Inner Tracker modules differs from the TT design. The silicon sensors and readout electronics

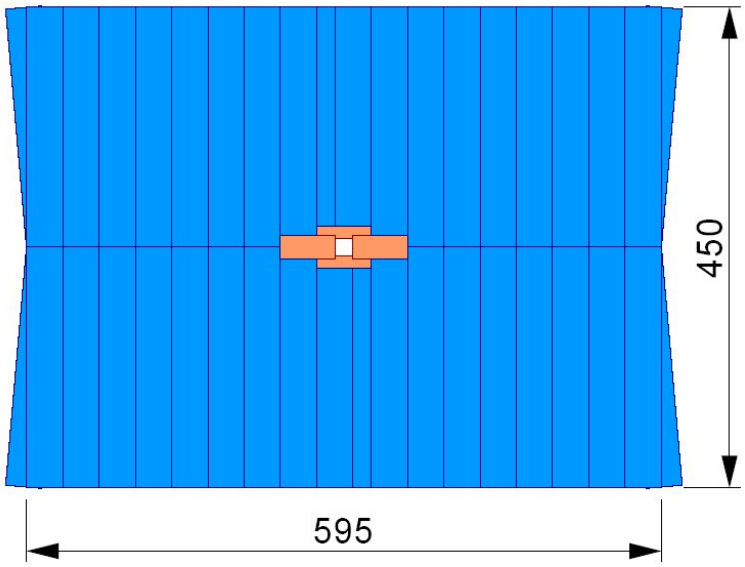

Figure 4.4: Drawing of one of the tracking stations T1-T3 (from [13],dimensions in cm). The outer regions with low particle densities are covered by the Outer Tracker while the area around the beampipe is read out with the Inner Tracker.

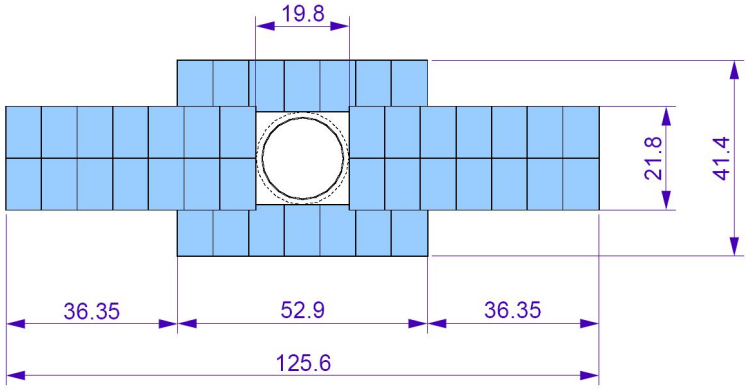

Figure 4.5: Detailed view of one layer of Inner Tracker station T2. Dimensions are given in cm (from [13].)

are mounted onto a sandwich structure support plate, which consists of an isolating polyimide layer and two carbon fibre sheets, separated by 1 mm of Airex^{TM} foam. Figure 4.6 shows an expanded view of a two-sensor module for the Inner Tracker.

Compared to the Trigger Tracker, the readout strips of the Inner Tracker are shorter and have therefore a lower capacitance. To minimize the amount of material inside the detectors acceptance, thin silicon sensors were chosen, which generate still enough signal to obtain a sufficiently high signal-to-noise ratio. Table 4.2 summarizes the sensor thicknesses and associated strip capacitances of the IT one- and two-sensor modules. Again, 3 pF are included to take the capacitance of the pitch adapter and the bond wires into account.

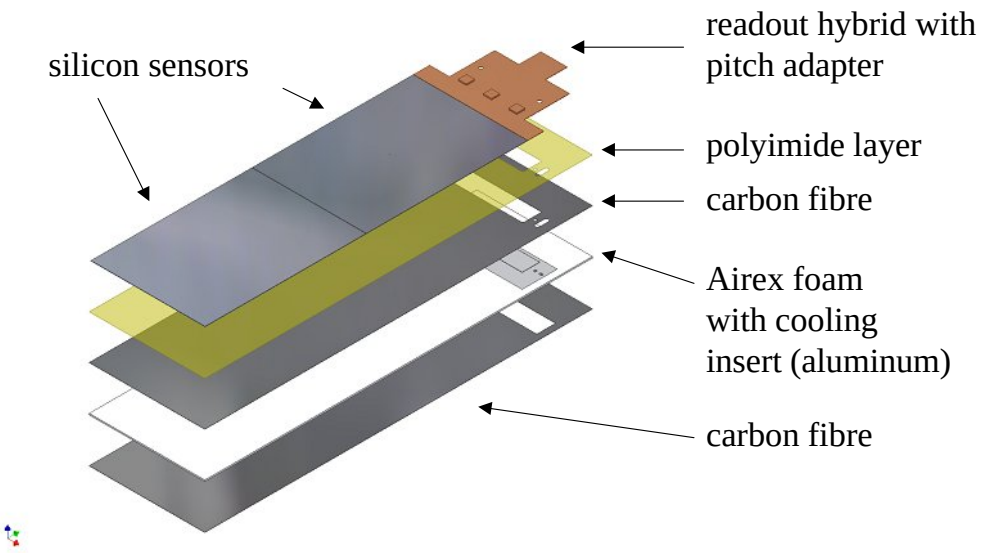

Figure 4.6: Expanded view of a 2-sensor module for the IT station (taken from [15]).

Table 4.2: Total strip capacitance for the IT sensor modules including 3 pF to account for the pitch adapter and the bond wires.

number of sensors	sensor length [cm]	sensor thickness [μm]	total strip capacitance [pF]
1	11.0	320	22.5
2	22.0	410	40.0

The active silicon area of the Inner Tracker is 4.13 m^2 with 336 readout sectors of 384 strips each. The results in a total number of 129024 channels.

Chapter 5

The Beetle Readout Chip

The Beetle readout chip [16], designed by the ASIC-laboratory of the University Heidelberg, is used for the readout of the silicon strip detectors. This chapter describes the basic chip architecture and the performance of the chip version 1.3 (shown in Figure 5.1), which will be used for all LHCb Silicon Tracker stations. The influence of its performance on the subsequent digitization of the detector data will be discussed as well.

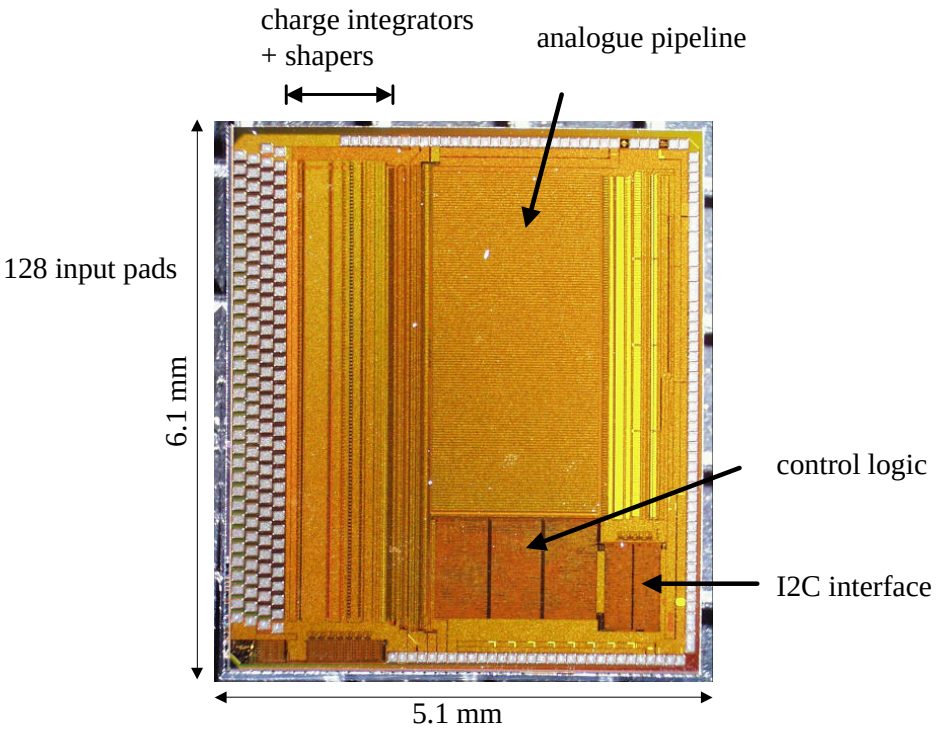

Figure 5.1: The Beetle readout chip.

5.1 Chip Architecture

The Beetle is a 128-channel charge integrator, with a tunable shaping time of the order of 25 ns. It is designed and produced in 0.25 μm CMOS technology, which was radiation hardened by employing specific layout and design techniques. A basic block diagram is shown in Figure 5.2.

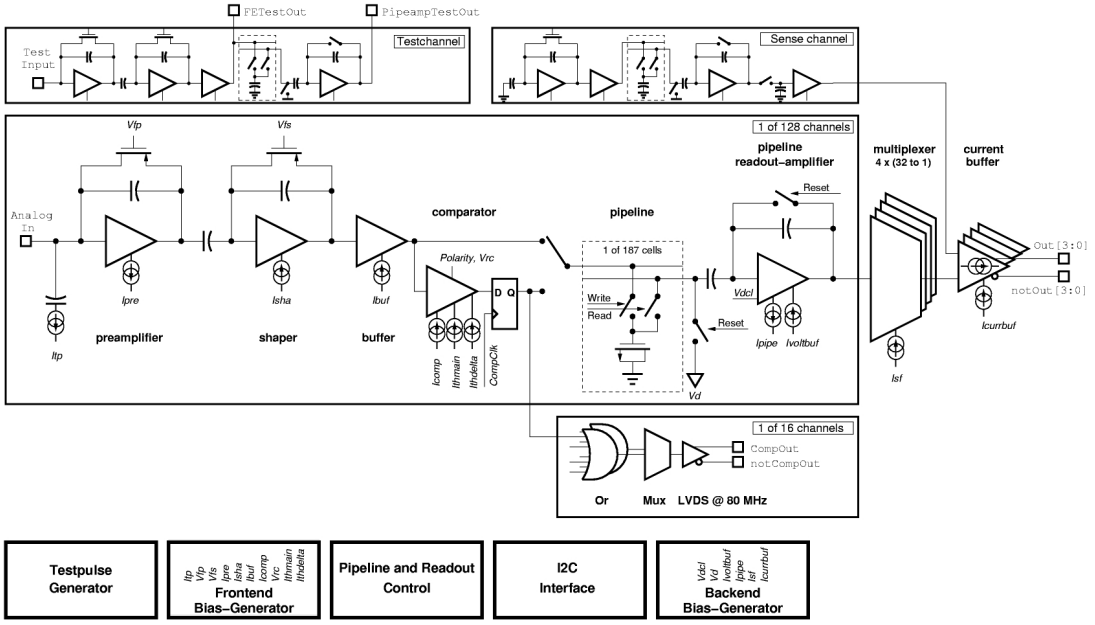

Figure 5.2: Schematic block diagram of the Beetle readout chip (from [16]).

Charge signals from the connected silicon sensor are integrated and shaped in the analogue frontend before being sampled every 25 ns into the analogue pipeline memory of the Beetle. Here, the charge information for each channel of the last 160 bunch crossings is stored to ensure a deadtime-free readout. Upon a Level-0 accept signal from the trigger electronics, the Beetle reads the analogue information stored in the pipeline. The exact position of the corresponding event in the pipeline is determined by the fixed timespan needed for the trigger decision and can be programmed with the latency register of the Beetle. The 128 channels are multiplexed into 4 output ports with 32 analogue values of 25 ns duration each. Additional information, for example the read out pipeline position, are encoded into four header bits per port. Per port, the output has therefore a total length of 36 values of 25 ns each. Hence, the resulting data frame of 900 ns length is compatible with the maximum Level-0 accept rate of 1.1 MHz, as specified in [9]. A binary signal (*DataValid*) is sent in parallel to facilitate the synchronization of this analogue data frame. The duration of this signal is shortened by one clock cycle to 875 ns to provide a signal gap even for consecutive readouts and starts one

clock cycle (25 ns) earlier than the analogue readout to allow a possible setup of subsequent processing stages. The analogue readout mode is used by the Vertex Locator and the Silicon Tracker. The Beetle also includes the option of a full binary readout, which is used by the Pile-up Veto detector. The analogue outputs are designed as fully differential current drivers, capable of driving several meters of impedance controlled differential lines. The differential outputs as well as all fast digital inputs are designed as LVDS interfaces to minimize EMI[1]. Several on-chip parameters, like shaping time, can be set by register-programmable digital-analogue converters, which can be accessed by an industry-standard I2C bus [17].

Different versions of the Beetle were produced during its development. The Beetle 1.0, submitted in April 2000, was the first version of the complete readout chip, but had a bug which prevented its registers from being programmed. This bug was fixed in the follow up version 1.1 (March 2001). The chip version 1.2, which was submitted in April 2002, included for the first time a triple-redundant control logic and an improved frontend. The Beetle 1.3 (June 2003) reduced the clock noise, which was present at the output of the chip version 1.2 and featured an enhanced analogue output driver. As the Beetle 1.3 satisfied the requirements of the Silicon Tracker, it was chosen for its series production. For a complete version list, see [16].

5.2 Performance of the Beetle Version 1.3

One of the important issues of the Beetle performance is the noise, which is mostly dependent on the design of the preamplifier stage. As shown in Section 3.1.2, the amplifier noise depends linearly on the detector's capacitance. The determination of the slope and offset was initially performed on the BeetleFE chip, which was a prototype incorporating several frontend designs on a single die. In addition, other parameters relevant to this work are presented here. Further information on the Beetle chip can be found in [16].

5.2.1 Amplifier Noise

In the prototyping stage of the Beetle, it was decided to produce a reduced prototype chip incorporating several frontend designs, which were under review for use in the full Beetle readout chip. This *BeetleFE* chip only included 12 preamplifier/shaper pairs for direct comparison against each other. Those frontends differed in their geometric size, their biasing and the value of the feedback capacitance. Bias currents and voltages were supplied by a second chip called *BeetleBG*. Both chips were placed close to each other on a single prototype board for characterization, as shown in Figure 5.3. By characterizing the noise dependence on the main four parameters of the frontend (bias currents and feedback resistances of preamplifier and shaper), a set of default parameters for low-noise operation was defined.

[1] EMI: electromagnetic interference

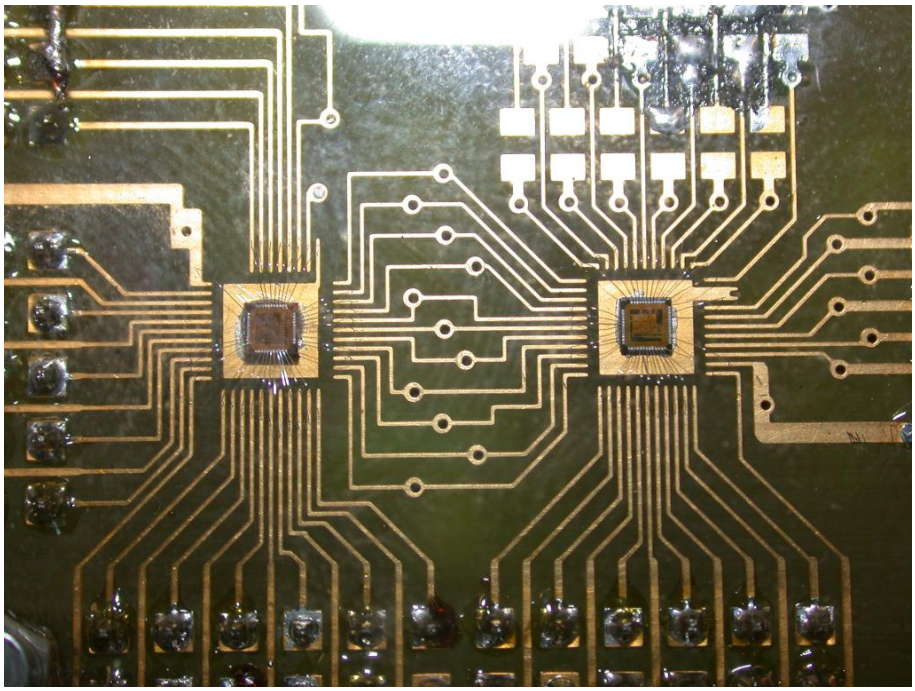

Figure 5.3: Test board of the BeetleFE11 (right) with the BeetleBG (left).

The gain of the different frontends was determined by injecting a known charge and measuring the response of the preamplifier-shaper combination. This was realized by applying a known voltage step to a known capacitor. The introduced charge can then be calculated by using $Q = C \cdot U$. To simulate the mean charge loss of a minimum-ionizing particle in 300 μm of silicon, a voltage step of 3.5 mV was applied to a capacitor of 1 pF, injecting a charge of 3.5 fC into the frontend. With this calibration, the noise of the preamplifier-shaper combination could be characterized for different externally applied load capacitances.

As a result, the frontend showing the best performance concerning noise, remaining signal 25 ns after the peak signal and saturation was chosen for use in the Beetle from version 1.2 on. This noise measurement was performed independently at the ASIC laboratory, at NIKHEF and at the University of Zürich, using different setups and analysis tools. The results of the three measurements are in excellent agreement with each other, as shown in Figure 5.4. The measurements resulted in a combined ENC of 451 $e^- + 46.8 \frac{e^-}{pF}$. The noise performance was found to be strongly dependent on the value of the shaper feedback, as a slower shaper restricts the bandwidth and therefore reduces noise. It is therefore possible to reduce the noise at the cost of a longer detector pulse.

A final characterization of noise for the complete Beetle 1.3 was performed as well. The ENC is shown for different setting of shaper feedback voltage in Table 5.1. Although slightly higher than the measured ENC for the frontend alone, this is considered to be in good agreement as additional elements in the full Beetle chip contribute to the overall ENC.

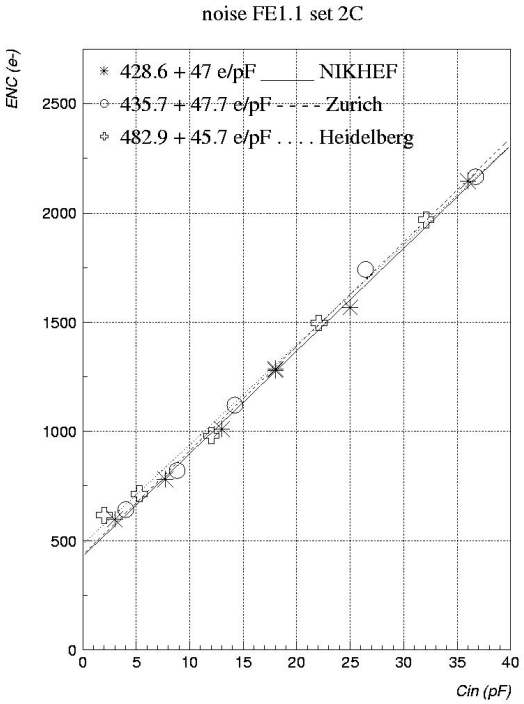

Figure 5.4: Noise measurements for the BeetleFE11 chip.

Table 5.1: Measured ENC for the Beetle 1.3 for different shaper feedback settings V_{fs} (taken from [16]).

V_{fs} [mV]	Equivalent noise charge
0	$ENC = 547.7e^- + 52.64e^-/pF \cdot C_{in}$
100	$ENC = 539.1e^- + 51.89e^-/pF \cdot C_{in}$
400	$ENC = 542.8e^- + 49.38e^-/pF \cdot C_{in}$
1000	$ENC = 465.1e^- + 45.22e^-/pF \cdot C_{in}$

For large detector capacitances, an increase of V_{fs} from 0 mV to 400 mV results in a 6% decrease in noise. In parallel, the remaining signal 25 ns after the peak signal is increased from 24% to 34% for a load capacitance of 25 pF [19].

5.2.2 Dynamic Range

The Beetle 1.3 can linearly amplify input charges of ± 110000 e^- with the saturation being reached at about ± 200000 e^- [18]. These numbers were measured without external load capacitance and are limited by the capacity of the cells of the Level-0 derandomizer pipeline.

The gain of the preamplifier is reduced for increased load capacitance. Therefore a signal equivalent to a higher charge can be stored in the pipeline cells of the Beetle. The measured gain decreases by about 45% for a load capacitance of 50 pF compared to the gain without

load capacitance [19]. Therefore the linear range is increased to about ±200000 e^- for such a detector capacitance, with saturation being reached at about ±370000 e^-. For a sensor thickness of 500 μm, this corresponds to ±5.4 and ±10 times the most probable signal of a MIP, respectively.

Table 5.2 shows the linear dynamic range for the different sensor thicknesses and ladder capacitances used in the Silicon Tracker. The given capacitances are not directly related to the sensor thicknesses. Thicker sensors with their larger signal can be used to build larger detectors with higher capacitance and therefore increased noise.

Table 5.2: maximum input charge for linear amplification for Beetle 1.3.

silicon thickness [μm]	MIP charge [e^-]	detector capacitance [pF]	gain (rel. to 3 pF)	lin. dynamic range [MIP]
320	23800	22	0.72	±6.4
410	30500	40	0.62	±5.8
500	37300	40	0.62	±4.8
500	37300	60	0.50	±5.9

5.2.3 Power Dissipation

The power dissipation of the chip depends strongly on the operating conditions of the Beetle readout amplifier. Naturally, a device without any clock and all internal bias generators programmed to zero value will have little power dissipation, whereas a clocked chip with all bias generators set to maximum will have a large power consumption. As neither of the two cases is representative for the operation in the Silicon Tracker, a set of standard parameters, which represent a likely operational mode and a parameter set representing a worst case scenario have been defined (see [19] for actual parameters). Table 5.3 summarizes the nominal and maximum power dissipation measured per channel, per 3-chip hybrid (as for the IT) and per 4-chip hybrid (as for the TT). All values are given for 4-port readout, 40 MHz clock speed and a 1.1 MHz trigger rate, as expected for ST operation. The maximum current is calculated for the worst case operation parameters and serves as an input for the design of the power supply circuits and the cooling system for the IT and the TT stations.

Table 5.3: Power consumption of the Beetle 1.3 (taken from [19]).

parameters	power per channel [mW]	power per 3-chip hybrid (384 ch.) [mW]	power per 4-chip hybrid (512 ch.) [mW]	max. current @ 2.5 V [A]
normal operation	5.14	1974	2632	1.05
worst case operation	6.70	2573	3430	1.37

5.3 Implications for Data Digitization

The digitization of the data is done by converting the incoming analogue signal at regular time intervals into an integer number, using an analogue-to-digital converter (ADC). The precision of the conversion is defined by the digitization depth of the converter. For example, an 8 bit digitization has a range of $2^8 = 256$ possible values.

The overall signal amplification in front of the ADC has to be large enough, so that the frontend noise present at the input of the converter is larger than its internal noise. If the gain is too low, the quantisation noise of the ADC will dominate and possibly mask weak signals. On the other hand, the higher the gain is set, the larger the number of strong signals that will drive the ADC into saturation, therefore reducing the maximum linear signal that can be recorded. The dynamic range can be increased by using a higher digitization depth, but this results in a larger amount of digital data, a higher power dissipation and an overall increase of the systems cost. Therefore, a good knowledge of both signal and noise is important to decide on the required digitization depth.

The minimum detector capacitance encountered in the Silicon Tracker is of the order of 10 pF, which corresponds to a minimum noise of about 1000 e^-. The maximum signal is generated by 500 μm thick silicon, with a most probable value of 37300 e^- per MIP. Due to statistical fluctuations of the energy loss in the silicon detector, the actual energy deposited by a single particle may also be several times larger. As the Beetle readout chip is linear up to an equivalent charge of about 5 MIP, the ADC range should be matched to this value. Simultaneously, the frontend noise should be larger then the ADC quantization noise U_{noise}, which is:

$$U_{noise} = \frac{U_{LSB}}{\sqrt{12}} = 0.288 \cdot U_{LSB}$$

U_{LSB} is the equivalent voltage difference of the least significant bit (LSB) of the ADC. To ensure that the frontend noise is significantly larger than this quantization noise, the amplifier gain is set to produce a frontend noise of $2 \cdot U_{LSB}$ in the ADC. For reliable hit finding in the analysis, a typical MIP signal should have a minimum Signal-to-Noise ration of at least 12, which requires a MIP signal of at least $24 \cdot U_{LSB}$. The 5 MIP dynamic range would be equivalent to $120 \cdot U_{LSB}$. This would result in a minimum digitizing depth of 7 bits ($2^7 = 128$ values). While the physics signals from traversing particles generate only unipolar charge signals in the Beetle, the superimposed common mode noise affecting all inputs of one Beetle in phase is bipolar and has ideally a gaussian distribution. To prevent this common mode noise from saturating the ADC, the Beetle baseline is placed in the middle of the ADC input range. To keep the required 7 bit range for the Beetle signal, the total digitization depth has to be 8 bits. This also fits to standard commercial components for data acquisition and processing.

5.4 Readout Hybrid

The readout hybrid is the basic electronic module for readout of the silicon strip detectors. It is constructed in multilayer technology with polyimide as carrier material. This allows for a feature size of 50 μm, which simplifies the layout. The hybrid has a different design for the two sections of the Silicon Tracker. An Inner Tracker readout hybrid carries three Beetle chips for a total of 384 readout channels. A readout hybrid for the Trigger Tracker hold four Beetle chips with a total of 512 readout channels. The number of channels is therefore identical to the number of strip of the according silicon strip detector. A ceramic pitch adapter is used to convert the input pitch of the Beetle chips to the strip pitch of the sensors. A picture of an IT readout hybrid is shown in Figure 5.5.

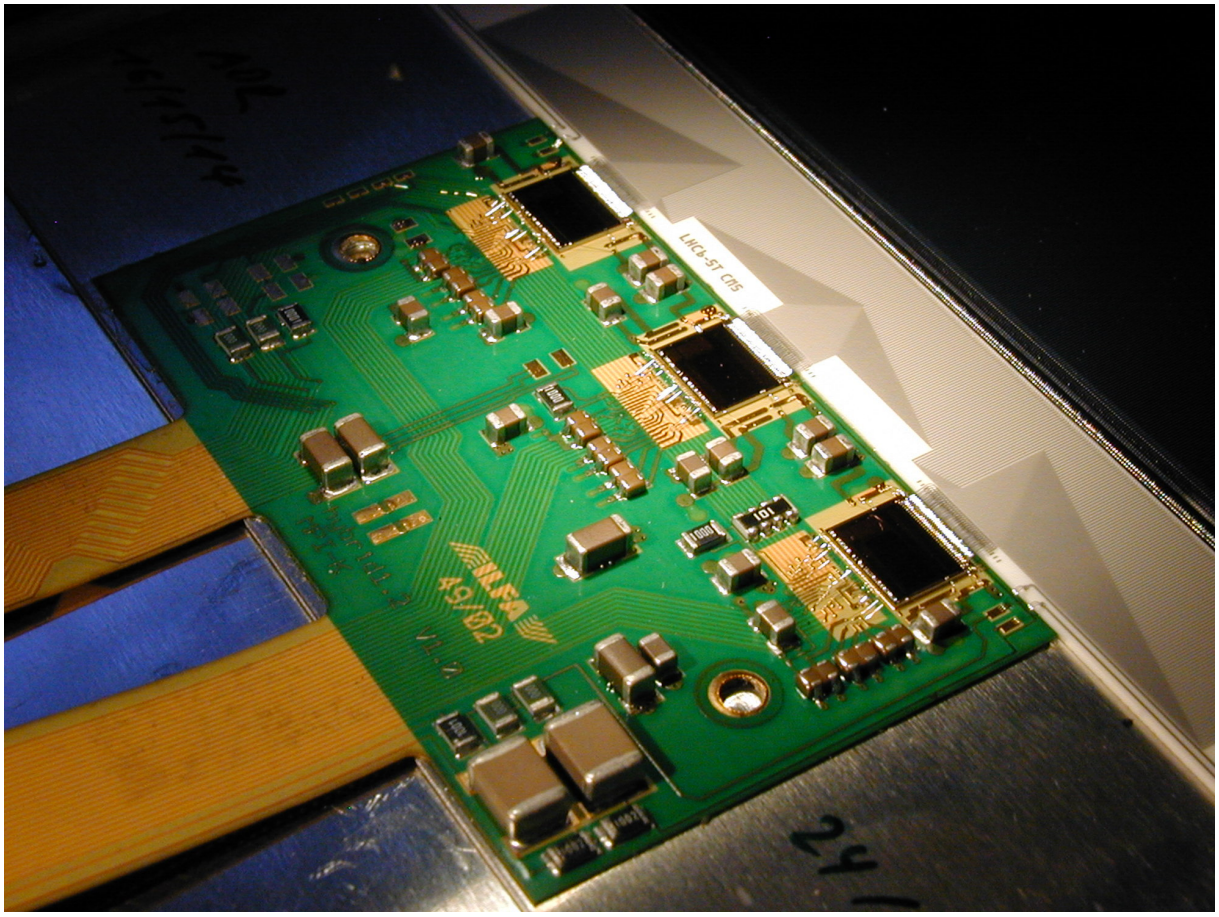

Figure 5.5: Photo of an assembled IT readout hybrid.

As the readout hybrid is located close to the beampipe and therefore experiences high fluences of ionizing radiation, only radiation-hard components are allowed here. As a result, the Beetle chips are the only active devices on the hybrid. Other components are the blocking capacitors to stabilize the supply voltages an internal nodes of the Beetle chips and resistors for line termination. In addition, a filter for the sensor bias voltage is included on the hybrid to suppress high frequency contents on the high-voltage line.

Chapter 6

Overview of the Data Readout System

This chapter discusses the general scheme used for the transmission of the large amount of data produced by the Silicon Tracker. After summarizing the requirements imposed by the Silicon Tracker, the different transmission systems used in this approach are discussed.

6.1 Requirements of the LHCb Silicon Tracker

With parts of the Silicon Tracker contributing to the Level-1 trigger decision, readout of the complete detector has to be compatible with the maximum Level-0 accept rate of 1.1 MHz. Additional parameters, which define the requirements to the Silicon Tracker readout system are shown in Table 6.1. The total number of readout strips for the Silicon Tracker is 272384, which results in an equivalent of 8512 analogue channels, taking into account the 32-fold multiplexing of each Beetle output.

Table 6.1: Requirements to the LHCb Silicon Tracker readout system.

	Trigger Tracker	Inner Tracker	total
Number of silicon sensors	896	504	1400
Number of sensor channels	143360	129024	272384
Number of readout hybrids	280	336	616
Number of Beetle amplifiers	1120	1008	2128
Beetle analogue output channels	4480	4032	8512
avg. trigger rate	1.1 MHz		
Digitization depth	8 bits		
net physics data rate	1.43 Tbit/s	1.29 Tbit/s	2.72 Tbit/s
physical transmission distance	up to 100 m		
max. total ionizing dose	$<$ 15 krad (10 years)		

6.2 Overview of Proposed Data Readout System

A digital optical transmission technology was chosen for transporting the Silicon Tracker data from the detector to the counting house. The decision was based on the availability of components and the reliability of such a system. In addition, due to increased demand on the commercial market, many of the components proposed in the design are getting more and more common on the fibre technology sector and this reduces the risk for individual components to become obsolete soon. An overall view of the proposed system is shown in Figure 6.1.

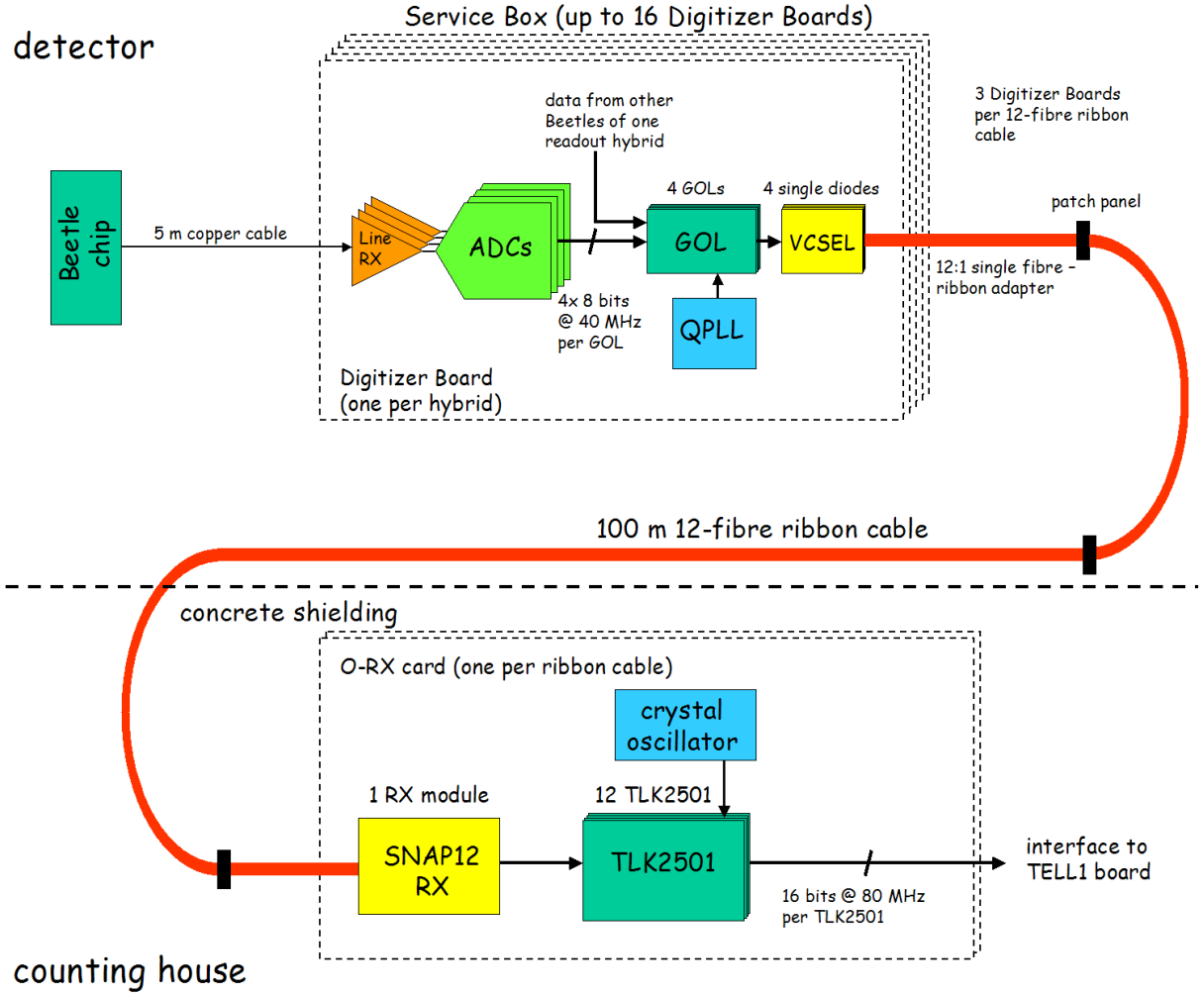

Figure 6.1: Block diagram of the Silicon Tracker readout system. The numbers are given for the readout of a TT hybrid.

The Beetle readout hybrid is connected with a copper cable of 5 m length to the ADC, which digitizes the analogue data at a sampling rate of 40 MHz. The digitization is performed in a so-called Service Box, that is housing all on-detector electronics aside from the readout

hybrid itself. The separation of the Service Box from the hybrid allows to place it outside the acceptance of the detector. The location of the Service Box is also important for the electronic components, as the expected radiation doses drop with increasing distance from the beampipe. This significantly reduces the requirements for radiation qualification of the used components.

The digital data is encoded by a gigabit optical link serializer, which directly modulates the output of a laserdiode. The complete data processing from digitizing until transmission into the fibre is done in the Service Box. While each laser diode couples to a single fibre, the cabling for the long distance is done with 12-channel ribbon fibre. In the counting room, this is inserted into a multi-channel optical receiver module. This module is located on the optical receiver card (*O-RX card*), an element of the Level-1 preprocessor unit (*TELL1*) both described in Chapter 11.

In the following sections, the short analogue copper transmission in front of the ADC and the digital optical transmission for the long distance transmission is discussed.

6.3 Analogue Copper Transmission before Digitization

The transmission of electrical signals with copper wires dates back to the 1830s, when first tests in Germany performed by Gauss and Weber demonstrated the technology. The invention of the Morse-Code by Samuel Morse in 1844 provided the ground for the development of widespread telegraphy networks. Electrical signal transmission with wires can be categorized into two main classes: unipolar or differential signaling. In a unipolar signaling scheme, one signal wire is used together with a ground wire. Depending on the type of transmitted signal, the ground wire serves as a voltage reference, if the voltage is used as a signal or as a return path for the current, if the current is used as a signal. While voltage-signalled systems are simpler in realization, the trend in modern wired high-speed transmission is to use current signals, as the received signal is independent from any contact resistances. When using multiple signals in parallel, only one ground wire is needed in principle, which keeps the number of signal wires down. However, any contact resistances in conjunction with current flowing on this ground wire will result in a potential difference (called ground bouncing) between the ground levels of the transmitter and the receiver, which can lead to transmission errors.

This problem is avoided by using the differential signaling scheme. As the name implies, in differential transmission the potential difference between two signal wires is used for the data transmission. A ground line is still needed between the transmitter and the receiver to keep the mean voltage of the differential signal pair, the common-mode voltage, within the receiver's input range. Here, ground bouncing is much smaller than in unipolar signaling because the ground connection does not carry any signal current. Another benefit of the differential transmission is its rather high immunity against external pickup, as both wires of the differential signal pair are usually routed close together. Hence, any induced pickup will have the same size and polarity on both lines. It therefore does not appear in the subtracted

signal as long as the external noise fits into the input range of the differential receiver. The Beetle readout chip therefore uses a differential current driver as analogue output.

The Beetle transmits one analogue value every 25 ns. Cable capacitances in combination with the limited current drive capability of the Beetle output limit the risetime of the signal. This results in an extended duration of the rising edge, where digitization of the analogue value is not possible. The analogue transmission medium should therefore be optimized to conserve as much as possible of the 25 ns signal duration by reducing the risetime. As the Beetle output drive strength is given, this can only be accomplished by minimizing the cable capacitance. Industrial standard twisted pair cables are able to fulfill this requirement, having a typical characteristic capacitance of only 43 pF/m.

Commercially available SCSI-3 cable of 5 m length was chosen to connect the readout hybrids to the Service Boxes. Including 34 signal pairs, they provide enough lines to provide all necessary signals for a readout hybrid, including the supply voltage. Channel-to-channel skew and variation of the impedance are minimized due to the optimization onto the target application, which are fast information technology interconnects. In addition, the SCSI-connectors are widely available, removing the necessity to use a proprietary high-density connector. Future maintenance and replacement is therefore simplified.

6.4 Digital Optical Transmission after Digitization

The first optical fibres were developed in 1970 by Keck, Maurer and Schultz for Corning Inc. [20]. Their light transmission capability is based on the total reflection of light at the boundary between two media with different refractive indices. They are produced by covering a thin glass fibre with a cladding of lower refractive index. The light then propagates by repeated reflection inside nthis fibre channel.

The data is encoded into the amplitude of the light signal by modulating the light output of a diode connected to one end of such a fibre. Photodiodes are used at the receiving end to recover the data. The operational wavelength is chosen to be close to the dispersion minimum of the fibre to minimize the spreading in time of any signal during transmission. In addition, the optical attenuation of a fibre is also a function of the wavelength. The commercially mostly used wavelength regions are located at 850 nm and 1310 nm, where both requirements are met, depending on the exact fibre type.

The big advantage of optical data transmission is their high immunity to electromagnetic interference and the inherent galvanic decoupling of the transmitter and the receiver. With typical cable diameters in the order of a few mm, which is mainly dependant on the cable armor rather than on the transmission medium itself, the optical fibre is able to transmit orders of magnitude more information for the same cross section used.

Bandwidths of 500 MHz over a length of 1 km are common for fibres with a core diameter of 50 μm and a cladding outer diameter of 125 μm. Even higher bandwidths are possible by

reducing the number of possible propagation paths in the multimode fibre by reducing the core diameter to 9 μm, as shown in Figure 6.2. The resulting singlemode fibre only allows a single propagation path inside the medium and therefore reduces the so-called *modal dispersion*. Typical bandwidths are between 2 and 5 GHz for 1 km. Despite the better performance of singlemode fibre, multimode fibre was chosen for the Silicon Tracker readout, as the larger core diameter simplifies alignment during production and therefore reduces the cost of the fibre cable significantly.

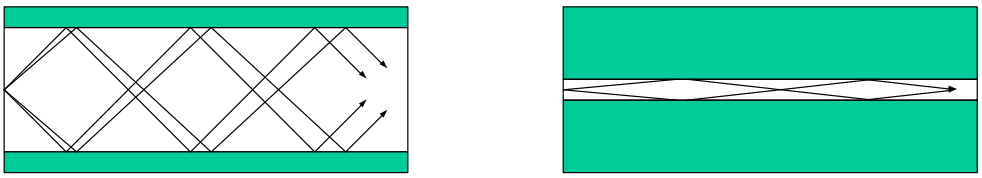

Figure 6.2: Light propagation in multimode fibre (left) and singlemode fibre (right).

Digital rather than optical transmission is used for the LHCb Silicon Tracker. This approach was mainly driven by cost considerations and the availability of the GOL serializer, which is a radiation hard gigabit serializer developed by the CERN microelectronics group [21]. The digitized data coming from the ADC is serialized into a high-speed datastream, which is used to modulate a laserdiode. In this way, the large bandwidth of the fibre is used much more efficiently than by using analogue transmission, where one fibre is needed per analogue signal. In the presented design, one GOL serializes data from four ADCs, which digitizes the four analogue output signals from one Beetle frontend amplifier.

Another key aspect of the digital data transmission is the highly reduced cable cross section, that is needed to transport the data. This is illustrated by a comparison of the cross section of the analogue transmission copper cables in front of the ADCs with that of the optical links between the Service Boxes and the counting room. For each readout hybrid, one multi-wire cable is needed. For the whole Silicon Tracker, this sums up to 616 cables with a diameter of 9 mm each. The total copper cable cross section is therefore $616 \cdot 0.64$ cm^2 = 394 cm^2. The actual cross section occupied by the cables is higher due to imperfect packing of the round cables. When using optical fibre, one optical fibre per Beetle is needed, resulting in 2128 fibres in total. For single fibre cables, we assume an outer diameter of 2 mm, which leads to a total cross section of $2128 \cdot 0.031$ cm^2 = 66 cm^2. An even denser packing is possible by using multi-fibre ribbon cable, where 12 fibres are grouped into one cable with a individual cross section of 10 mm^2. This cable is also proposed for use in the Silicon Tracker and results in a cross section of $2128/12 \cdot 0.1$ cm^2 = 17.7 cm^2 which is less than 1/20 compared to the cross section of the copper cables used in front of the ADCs.

Another strong concern for an analogue copper readout system is the signal integrity. For a total length of 100 m, the transmission of fast analogue signals over copper cables is considered to be unreliable as the picked up interferences scale with the length of the cable. This argument is in particular valid in an environment such as the LHCb experiment, with

numerous sources of magnetic and electric fields ranging from lowest frequencies to several 100 MHz in spectrum. Together with the galvanic decoupling of transmitter and receiver section, this is a strong argument for choosing a digital optical scheme for transmitting the data from the Silicon Tracker to the counting house.

Chapter 7

Prototyping of Subsystems

7.1 Line Receiver and Analogue-to-Digital Converter

The purpose of the line receiver is to amplify the signal at the end of the terminated 5 m cable coming from the frontend amplifier to a level suitable for the following digitization. A high amplification is needed to maximize the signal while keeping noise low. However, care has to be taken not to set the amplification gain too high and drive the digitizer into saturation. These two boundaries set a window, in which the user can choose the amplification gain according to the physics requirements. In addition to the amplifier gain, the input and output voltage ranges have to be matched to the Beetle frontend chip and the analogue-to-digital converter (ADC), respectively. This can be achieved either by applying a voltage offset to the signal, using active components like transistors and operational amplifiers, or by using an AC-coupling, which can be implemented with a simple RC-highpass. While the latter solution has the disadvantage of cutting off of the transfer function at low frequencies, the benefits such as a low component count and exclusive use of passive, radiation tolerant devices makes this approach better for our application. The bias voltage for setting the offset of the AC-coupling can be derived from the following stage to ensure the signal is within the operating range of the according input. This is especially important for both the line receiver and the ADC.

The optimum setting of the ADC input bias voltage depends on the properties of the incoming signal. As common mode noise will be a significant part of the signal to be digitized, it has to be taken into account as well as the physics signal itself. While the latter has only positive polarity, when referred to the frontend chip's baseline signal, the common mode noise contribution is bipolar and randomly distributed around the nominal baseline. As the superimposed physics signal must not be driven into the saturation limit of the ADC, the best choice of bias would be a setting slightly lower than mid-range of the ADC's input range. To maintain the optimum coverage of the bipolar dynamic range of the Beetle, it was nevertheless decided to center the Beetle baseline inside the input range of the ADC.

The next parameter to be fixed is the gain of the line receiver. As discussed in section

5.3, a full range equivalent to a charge signal of ±5 MIP should be adequate for the Silicon Tracker to overcome the internal noise of the ADC while maintaining the ability to linearly process large signals. The best value for the gain of the line receiver would thus depend on the detector ladder, that will be connected to its input.

Since the gain of the Beetle frontend chip varies with the input load capacitance and the absolute value of a MIP charge signal depends on the sensor thickness, the line receiver gain would have to be optimized separately for each type of ladder. However, as the thicker sensors are assembled to longer detectors with higher capacitances, the resulting output pulse height per MIP remains almost unchanged, as the larger signal is partially compensated by a lower gain due to the higher strip capacitances (see Table 5.2). It was therefore decided to keep a uniform setting for the complete Silicon Tracker.

The device chosen as a line receiver is the Analog Devices AD8129 differential amplifier [22]. Being a true differential amplifier with an adjustable gain, its main benefit is the high bandwidth of 170 MHz at a voltage gain of 10. Due to the quasi-digital characteristic of the Beetle signal, which is an analogue signal binned at 25 ns, any bandwidth limitation reduces the duration of the flat-top of each bin, where the signal amplitude can be sampled properly. The actual gain setting of the amplifier is not implemented via the feedback resistor of the line receiver, as this device is optimized for operation at a gain of 10. To ensure stable operation, the gain of the receiver is fixed at 10 while the needed attenuation is set with a differential voltage divider, which is integrated into the 100 Ω line termination.

The differential signal at the input of the line receiver has also to fit into the input common mode voltage range, which is between 1.25 V and 3.7 V for the used 5 V operation. By design, the amplifier is capable to work with supply voltage ranging from unipolar +5 V to ±12 V bipolar. While the bipolar supply would lead to higher common mode input voltage range, the unipolar +5 V supply was considered as being sufficient for our design and chosen for simplicity of the overall circuit. AC-coupling is used here for the same reasons as explained earlier. The common mode noise which will be picked up by the 5 m copper cable coming from the frontend amplifiers will certainly be larger than the Beetle output signal itself, so a mid-range bias at 2.5 V provides maximum immunity against input saturation due to common mode noise. As the DC-component of the Beetle signal does not contain any information, this could be achieved by implementing a capacitive coupling of 100 nF per differential line, followed by a 1 kΩ resistor tied to the 2.5 V reference voltage. The resulting highpass has a time constant of $\tau = \mathrm{R} \cdot \mathrm{C} = 100\ \mu$sec. This is large compare to the typical length of the Beetle output frame of 900 nsec, so the shape of a 25 nsec long signal bin of the Beetle output will not be distorted, even for several consecutive active bins. If we assume the readout frame to be a positive step function of $t = 900\ ns$ duration, the deviation caused by the highpass at the end of the readout frame will be $\exp(-\mathrm{t}/\tau) = 0.991$, which means less than one percent deviation from a DC-coupled signal over the duration of one readout frame.

A general effect for AC-coupled systems is the dynamic shifting of baselines for signals with variable DC-components. When no hits are read out by the Beetle, its baseline can be treated as flat for this approximation. The Beetle header contains binary information, with its four bins being equivalent to ±30000 e− without load capacitance. We now take

the maximum occupancy on a single Beetle to estimate the expected baseline shift. Physics simulations show up to 5% strip occupancy for the innermost group of 64 readout strips of the TT station [23]. For a worst case assumption, we consider these hits to occur all on one readout port of a Beetle, which would translate into three active strips in a group of 32 strips. As another worst case assumption, we assume these three strips to saturate the analogue readout, which make them equal to a 5 MIP signal. As the Beetle header is also not symmetric, but being only about 1 MIP in size, we assume all four header bits to have the same polarity as the three saturated strips, but with a signal equivalent to 1 MIP. If we average all these contributions over the full readout frame of 36 readout bins, we end up with a baseline shift of just over 0.5 MIP, corresponding to a 10% shift compared to the full dynamic range of ±5 MIP of the readout. A shift of this order of magnitude is considered to be acceptable since the common-mode subtraction performed in the TELL1 board (see Section 11.2) is able to correct for it as long as the baseline is not driven into saturation.

To digitize the signal, the TSA0801 8 bit ADC from ST microelectronics will be used [24]. While ADC's with 8 bit precision have become very common on the market, the TSA0801 is special because it is fully constructed in deep submicron technology. Besides the advantage of a low power consumption of only 40 mW when sampling every 25 ns, the deep submicron design provides inherent radiation tolerance, which is critical for use in the LHCb environment.

A second shift of the DC-voltage has to be performed after the amplifier, as the following ATSA0801 has an internal reference fixed to 1 V. This second AC-coupling is achieved by a 100 nF capacitor followed by a 10 kΩ resistor connected to the reference. The time constant of this second highpass is even larger than the time constant of the first highpass, therefore causing no additional influence on the signal compared to the effects of the first AC-coupling. The ADC differential input range is 2 Vpp, which together with the differential amplifier gain of 11 and the input attenuator with a gain of 0.22 results in a true *differential* input range of 0.83 Vpp. This can be compared with the allowed *common mode* range on the input, which can be 2.45 Vpp and even higher for lower frequencies as a result of the AC-coupling lowpass. This gives the analogue input stage sufficient design margin to cope with high input noise.

Measurements were performed to test this configuration by connecting a silicon sensor with a Beetle 1.2 frontend hybrid via long copper cables to the AD8129 line receiver followed by the TSA0801 ADC. The prototype board is shown in Figure 7.1.

The performance of the line receiver was evaluated by connecting different cable types of up to 15 m of length between the Beetle frontend and the line receiver, while monitoring the signal at the input of the ADC [25]. Despite the presence of common mode noise of about 300 mV peak-to-peak, compared to a peak-to-peak Beetle header size of about 60 mV (which is equivalent to about 40000 e^- for 40 pF of load capacitance), the line receiver circuit was able to extract and amplify the detector signal out of the induced noise. The only visible effect, which distinguishes the different cables from each other was a decreased risetime of the signal, which correlated to the specific cable capacitance of the investigated cables. The most interesting result of this investigation was, that an unshielded twisted pair cable even outperformed a shielded of identical specifications, less the shielding. The obtained results

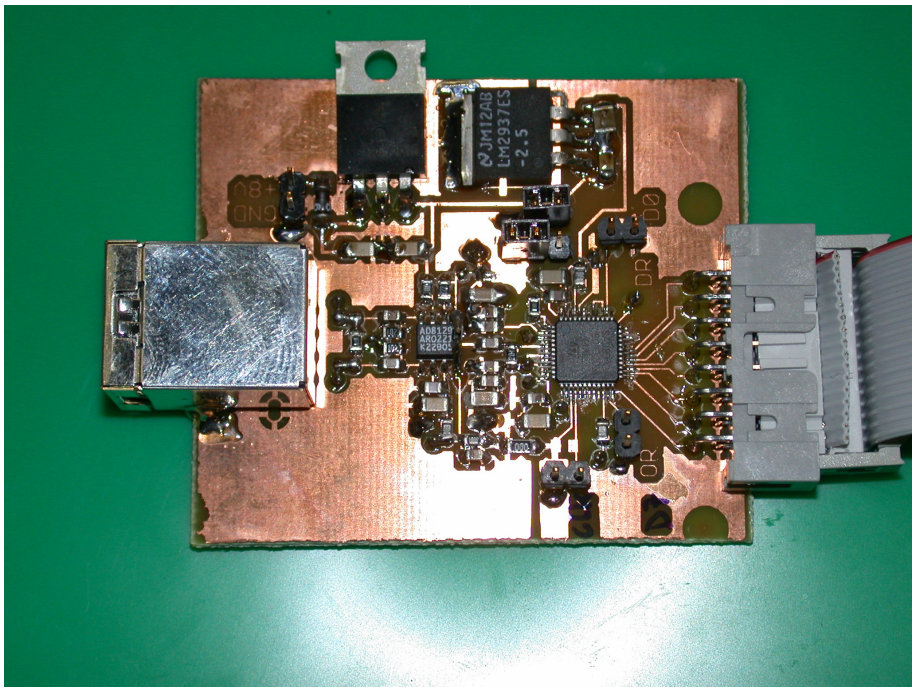

Figure 7.1: Prototype of the line receiver + ADC.

demonstrate the possibility to transmit the analogue data over a cable length of 15 m, albeit with no extra safety margin on the transmission quality. As this tests were done under clean laboratory conditions, the cable length for the detector installation is therefore limited to 5 m to include some safety.

The line receiver also introduces a high frequency compensation via the amplifier feedback to compensate for the finite bandwidth of the copper cable. By slightly increasing the gain for higher frequencies, it is possible to enhance the bandwidth of the cable and receiver, when viewed as a single system stage. This can be directly measured in the width of the flat top of a Beetle signal bin. Figure 7.2 shows the Beetle header afer 5 m of Category-5 twisted pair cable with the described line receiver. A width of 15 ns could be achieved, compared to an ideal 25 ns for infinite bandwidth. The ripple on this flat top is in the order of about 6 %, which leaves the option to use the full window of 15 ns for digitization. This relaxes the requirement on the actual timing of the signal sampling by the ADC.

A more detailed discussion can be found in [25].

7.2 Gigabit Serializer and Optical Transmitter

Following the analogue-to-digital converter, the parallel data has to be serialized and converted into an optical signal. This is done using the CERN GOL[1] chip [21], which has been

[1]GOL: gigabit optical serializer

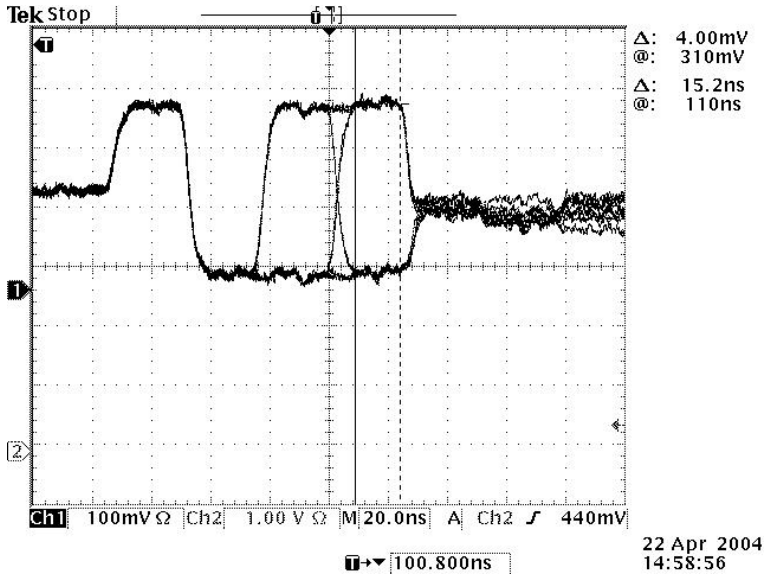

Figure 7.2: Header of the Beetle 1.3 after 5 m of twisted pair cable. The oscilloscope was used in persistence mode. The cursors are set to the edges of the flat top of the last header bin to measure its duration.

developed for the CMS experiment. For the Silicon Tracker readout, the so-called 'fast mode' with 8B/10B encoding option was chosen from the available GOL transmission modes. In 'fast mode', 32 bits are serialized at an input clock of 40 MHz, resulting in a total data rate of 1.6 Gbit/s. The 8B/10B encoding is the same as specified for ethernet data transmission [26]. It ensures DC-balance and a minimum number of signal transitions for the de-serializer to recover the clock from the transmitted data. It also provides control sequences to synchronize on the data frames and recognize transmission errors. Using an established transmission protocol permitted to select a commercial device for deserialization [27].

The serialized data can be supplied in two ways by the GOL chip. For transmission over longer board traces or for interfacing to commercial gigabit equipment, a CML[2] differential output can be used. For environments with higher ionizing radiation levels, the option to directly connect a plain VCSEL diode is provided via an internal laser diode driver.

The option of using multi-channel, parallel optical transmitter modules with integrated laser drivers was investigated since several large companies agreed on a common standard for multi-channel fibre optical modules, capable of being directly connected to a multi-fibre optical ribbon cable [28]. The price for such devices dropped to a competitive level when compared to discrete laser diodes. However, these modules use an integrated flash memory to store the bias settings for the laser array. These settings are programmed during production in the factory and are not available for the end user. The parallel transmitter approach was considered being too risky, as a single radiation induced single-event upset (SEU) could lead to the irreversible failure of an optical link and loss of its detector data. As a consequence, the possibility of using discrete VCSEL diodes was investigated. A prototype board with a

[2]CML: current mode logic

GOL 1.0 driving a single VCSEL in shown in Figure 7.3.

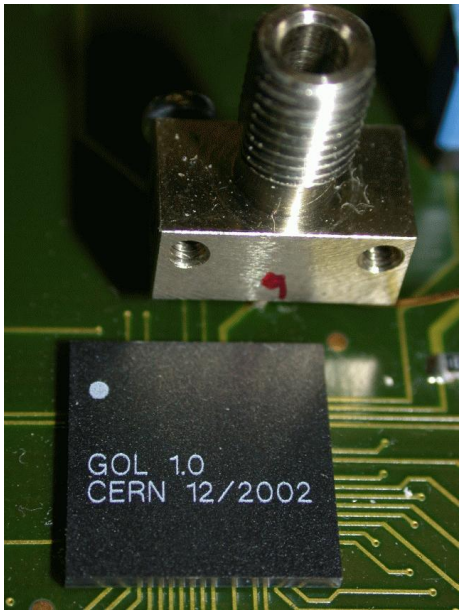

Figure 7.3: GOL 1.0 with VCSEL diode on a prototype board.

Although the GOL laser driver originally was designed to drive edge-emitting laser diodes (EELD), it is also compatible with modern VCSEL devices due to their low laser threshold current. However, it has to be noted that the GOL laser driver has a symmetric fixed current modulation of 10 mA around the adjustable bias current. The dynamic range of a laser diode is limited on the upper end by the maximum operating current, which is specified by the factory to achieve a given lifetime. Any increase beyond this current increases power dissipation and internal temperatures, leading to an early failure of the device. The lower limit of such a diode is the laser threshold current that is required for the laser effect to establish inside the device. Any current below the threshold current will lead to incoherent light emission, orders of magnitude below the rated laser output power. As the binary data is encoded via different power levels for '0' and '1', one might think of using a low bias setting to put the '0' state below the laser threshold. Theoretically, this would result in a clear separation of the binary states and good optical link performance. In reality, the laser power needs some time to settle to the programmed value. This turn-on/off times are significantly slower than the rise- and fall-times for continuous operation above the laser threshold. As a consequence, link performance would be poor, with effects ranging from reduced transmission speed to high bit error rate [29]. The VCSEL diode has to be compatible with the bias current range of the GOL and must sustain the 10 mA modulation without either going below the laser threshold or exceeding the recommended maximum operating current. Furthermore, the VCSEL device has to be able to produce the optical power required by the system design at a speed of 1.6 Gbit/s. In addition to those electrical and optical properties, the VCSEL device should ideally provide a direct interface to the optical fibre, and a receptacle which provides the mechanical fixture to the printed circuit board.

Two different VCSEL diodes were used during system prototyping. The first sample was a VCSEL from Honeywell Inc., type HFE4390-521 [30]. Later, a VCSEL from ULM-Photonics (type ULM850-05-TN-USMBOP, see [31]) was chosen in favour of the Honeywell VCSEL due to the included mechanical receptacle of the ULM-Photonics VCSEL.

7.3 Parallel Optical Receiver and Deserializer

The choice of the receiver for the optical signals is to a large extent determined by the optical transmitter, as it has to match its counterpart in terms of wavelength, speed and fibre type. However, the environmental requirements are less severe for the receiver due to its location in the counting room, where it is not exposed to radiation. As a result, commercial-off-the-shelf (COTS) components can be used to reduce cost and reliablity and simplify maintenance. Multi-channel receiver modules, compatible to the devices which were considered for the transmitting section are used here. The main benefit of using these modules is their availability on the market due to the SNAP12 standard [28]. In addition, the modules are rather small and dissipate only about 1.5 W of heat, which make them ideal to be used in densely packed DAQ crates. A sample module is shown in Figure 7.4.

Initial testing was performed with the PR2800 receiver from Paracer Inc. The preseries boards of the optical receiver cards are now equipped with MRX-9512 modules from Emcore Inc. [32] due to cost and availability reasons.

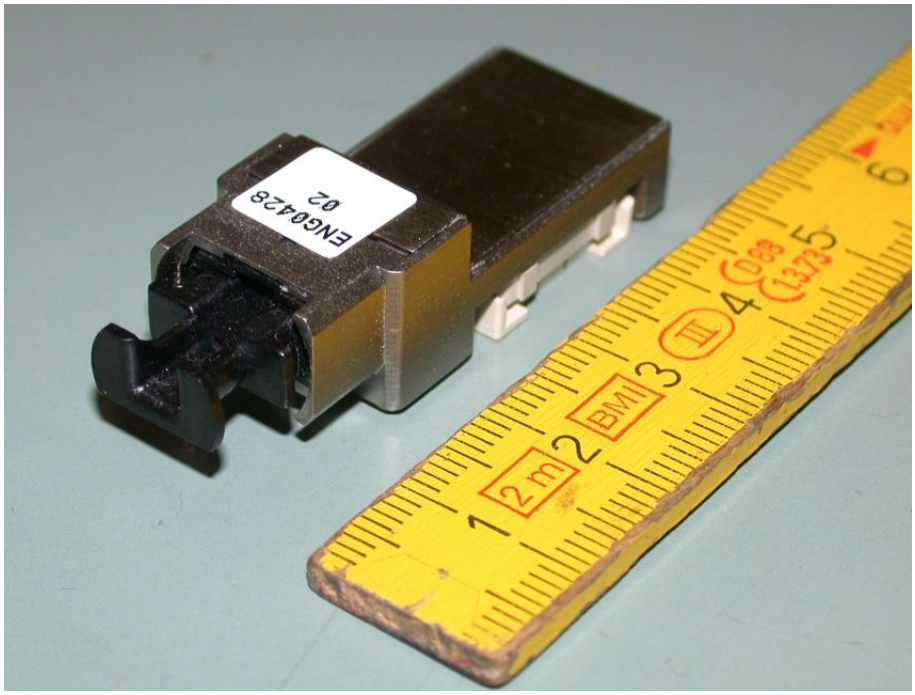

Figure 7.4: A SNAP12-compatible receiver from Emcore Corp.

The deserializer is the TLK2501 from Texas Instruments Inc.[27]. Again, no special precaution has to be taken when using this commercial device as at its proposed location, it is not subjected to radiation. The TLK2501 is designed to be compatible to the 8B/10B encoding of the GOL. A small FPGA for a second stage of demultiplexing is necessary as the GOL performs a 32:1 multiplexing at 40 MHz, but the TLK2501 decodes the data at double the clock frequency (80 MHz) with an output data width of 16 bits. A prototype serializer board, which is shown in Figure 7.5, was developed that carries a TLK2501 and a small FPGA to perform the demultiplexing of 16 bits to 32 bits, therefore restoring the original data format at the GOL input.

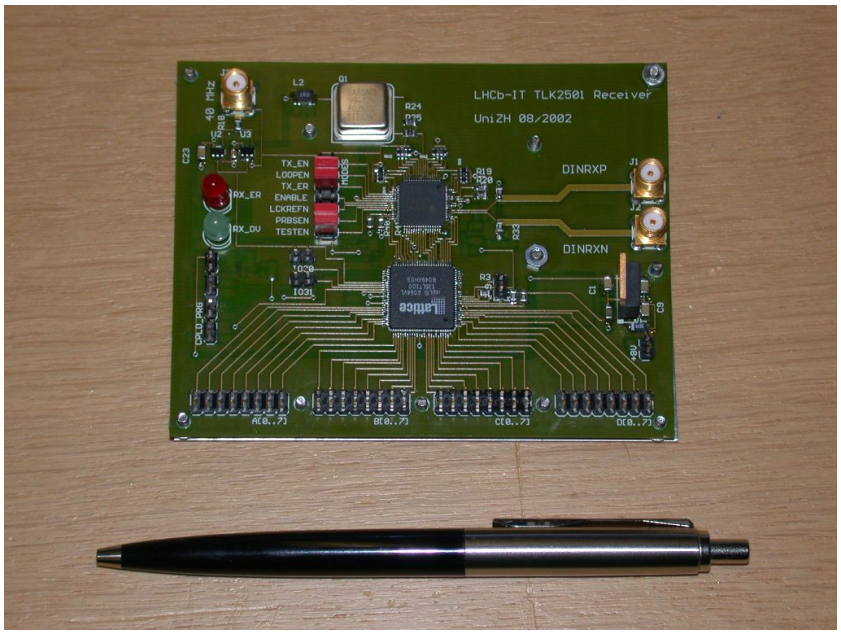

Figure 7.5: Prototype of a GOL-compatible deserializer.

Tests and performance of this board is described in Section 7.5.

7.4 Optical Fibre Cable and Connectors

The choice for the optical fibre is driven by the requirements of the transmitter and the receiver side of the optical link. Multi-channel fibre ribbon cable was the natural choice as can be directly plugged into the receiver. As this type of cable is widely used in information technology businesses and network wiring of recently built offices, cables produced from non-halogen materials are easily available. The optical fibre is provided by FOnetworks Inc.[33] and is a LSZH[3] type fibre, which is in compliance with CERN safety rules for cables. The use of non-halogen cable is a safety requirement from CERN [34]. A Kevlar strength member inside the cable increases the allowed pull strength, which is in particular important for installation,

[3]LSZH: low-smoke, zero-halogen

but also for later operation in high energy physics experiment. A recent development on the fibre cable market is a tubed version of this ribbon cable. To increase the fibre density even more, 8 ribbon cables are packed into a plastic tube, which provides even better protection for the fibres. The number of cables, which have to be installed also decreases by a factor of 8, saving time and money during installation.

The cables are equipped with SNAP12 compatible MTP interfaces, as shown in Figure 7.6, which provide the positioning of the fibres by precision pins in the ceramic ferrule. The flat polished surface of the ferrule also defines the reference plane for the MTP connector. The plugged connector itself is locked by a spring loaded collar, which has to be manually retracted for extraction from the mated connection. The connector mating is simply done by pushing it into the socket until the collar snaps in place.

Figure 7.6: Close-up of an MTP connector.

12-to-1 breakout cables are used to connect the single channel VCSEL transmitters to the multi-ribbon cable. Being equipped with an MTP connector on the multi-channel side, the breakout cables can be connected to the long cable section going to the counting room by a simple MTP-MTP mating interface. The single-channel side connector is a straight SMA connector, which can be directly locked into the VCSEL. As only stainless steel is used on both sides of this SMA connection, it provides a robust and secure lock of the fibre into the transmitter. Compared to other fibre connector standards like ST, FC or LC, which use plastic parts for their connectors, the SMA connection is less susceptible to damage and wear-out. The use of patch panels is planned to further reduce the risk of irrecoverable loss of optical links. Most fibre cable damage occurs at the cable ends, where cables typically have to be plugged repeatedly during the installation and commissioning phase and for detector

maintenance. Another possibility is excessive radiation damage, which may occur at the first few meters of the fibre, close to the detector. If a single long cable would be damaged in such a way, the cable could not be replaced, which would result in a permanent loss of the data link. The patch panels would be ideally located at easily accessible points in the counting room and in the cavern. Any fibre damage close to the transmitters or receivers can then be fixed by exchanging a rather short cable.

The current planning for the long cable part relies on a multi-ribbon tube, where 8 ribbons are grouped into one plastic tube with an 8-fold breakout into single ribbon cables on each end. A cross section of this cable is shown in Figure 7.7. This configuration has been shown to significantly reduce the overall cost, compared to single fibre ribbon. The commissioning work when routing the long cables in the experimental area is simplified. In addition, this multi-ribbon tube is more robust than a single ribbon, which further decreases the risk of damaging the optical fibre.

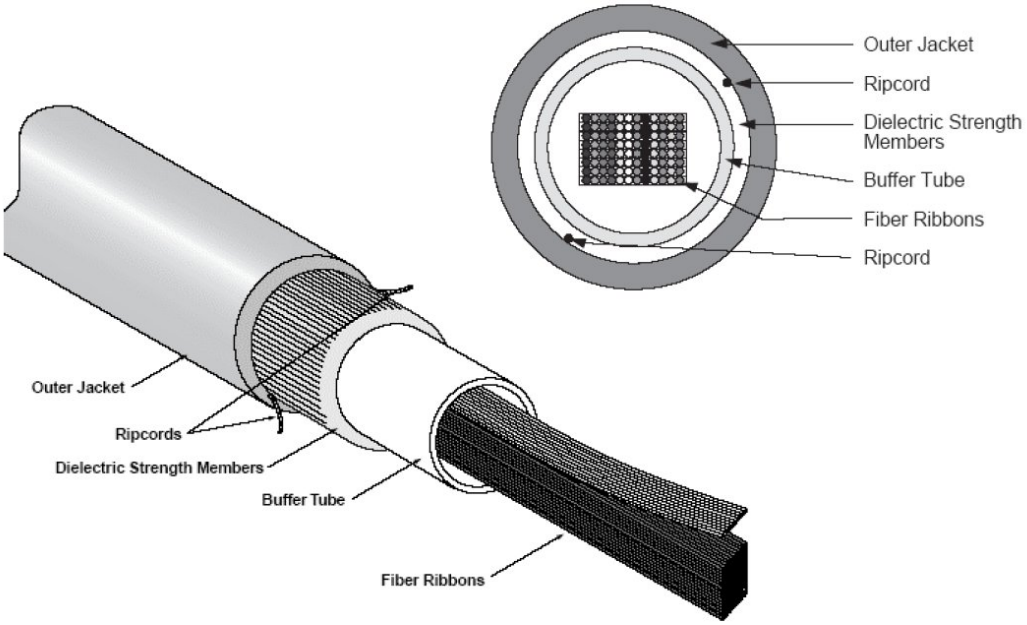

Figure 7.7: Multi-ribbon optical cable, used in the common LHCb optical links.

7.5 Verification of Prototype Performance

A digital bit error rate test would be the natural choice to actually verify the performance of the digital data transmission system. In such a test, a pseudo-random bit pattern is inserted into the system. The transmitted binary data is received and demultiplexed and then compared bit-wise with the original data. Any bit discrepancy is counted as an error and enters the calculation of the bit error rate:

$$BER = \frac{number\ of\ bit\ errors}{number\ of\ transmitted\ bits}$$

Typical achievable BER are of the order of 10^{-12}.

Although this approach seems to be fairly straight forward, its realization is complicated, since commercial BER test equipment is not accessible due to its prohibitively high cost. Consequently, alternative methods to evaluate the functionality and quality of the transmission system were studied.

A first indication for the quality of the transmission system is the determination of the eye diagram. For this, the serialized high-speed data has to be recorded by an oscilloscope, which is set to infinite persistence. To obtain a stable measurement, the trigger is connected to the transmission clock of the system. Generally speaking, the resulting picture is a superposition of the binary states ('0' and '1') which are transmitted over the serial line. For a perfect system, the transition edges between these states are infinitely steep, both states are perfectly defined and the time duration of a bit transmission, the unit interval, is perfectly stable. Figure 7.8 show effects that occur in a real system:

- limited rise-/falltimes
- clock jitter of the transmission
- variable levels for the binary states

The visible opening inside such a unit interval is commonly referred to as the 'eye', with the complete screenshot being called an 'eye diagram'. A wider opening of the eye characterizes a more robust data transmission system, while a small eye opening or even a completely close eye represents a poor transmission quality with a high bit error rate. A quantitative translation of eye closure into BER is however not possible as many aspects of the measurement setup would have to be included into the determination of the actual BER.

Figure 7.9 shows a recorded eye diagram from the prototype system. While some over- and undershoot effects are visible, the eye itself is wide open and free from state transitions. The transmission quality is therefore considered to be sufficiently good.

As further testing on the digital level was not possible, a 4-channel, 8 bit digital-to-analogue converter (DAC) capable of running at 40 MSPS[4], was used to convert the digitized data back to its original analogue form, which can be easily displayed on an oscilloscope. Any swapped connections would distort the original signal beyond recognition, so this setup is a fast confirmation of a proper association of data bits throughout the transmission system. As an example, Figure 7.10 shows the first Beetle output baseline, which was transmitted with the prototype system over a cable length of 98 m.

[4]MSPS: million samples per second

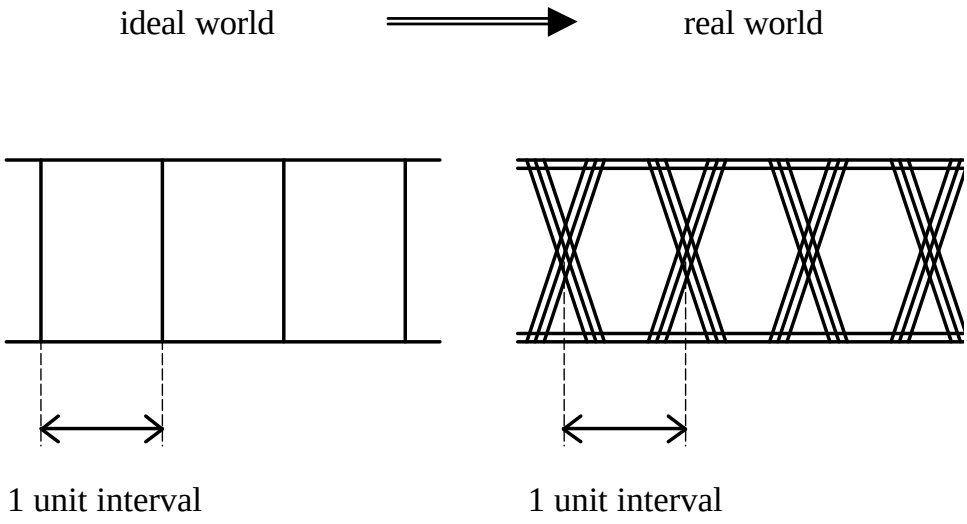

Figure 7.8: Eye-diagram of a digital transmission.

7.6 Optical Power Budget

The optical power budget between transmitter and receiver has to be designed to maximize the robustness of the system while staying within the limits of the used components. While a high optical power delivered by the laserdiode can be useful to compensate for aging effects in the transmission medium, the signal must not be so large that it saturates the receiver for nominal attenuation of the optical fibres. The maximum allowed input signal of the MRX-9512 receiver of -2 dBm combined with the nominal attenuation of the fibre cable of about 1 dB sets the maximum laser power to -1 dBm (0.8 mW). Typical and worst-case attenuation data for fibre cables and MTP connector interfaces are included to calculate a typical and a worst-case scenario for the optical power, that arrives at the receiver. The power margin can be calculated by combining this result with the receiver sensitivity, which is also shown in Table 7.1. Power levels are given in dBm, which is short for 'decibel referred to 1 mW'. Attenuations are given in dB, which allows to sum up dBm and dB.

The worst-case power margin of 9.0 dB (equivalent to a factor of 8) provides a large safety margin to cope with component tolerances. In addition, the power margin allows for some additional fibre attenuation, which may be induced by radiation. Moreover, the fibre cables which are closest to the detector are replaceable to add even more reliability to the system (see also Chapter 12).

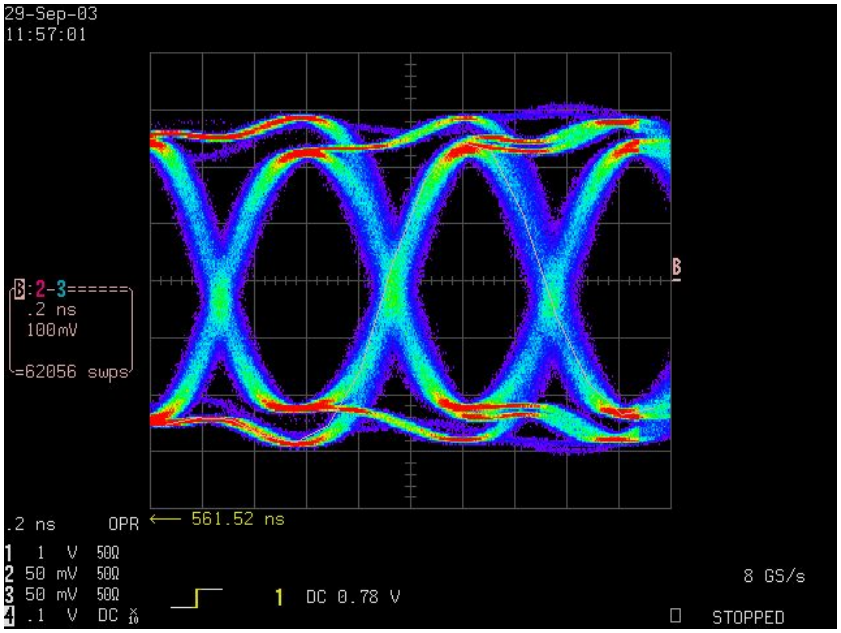

Figure 7.9: Eye-diagram of the optical signal, recorded after 90 m optical fibre.

Table 7.1: Typical and worst-case power budget for the proposed optical readout system.

	worst-case	typical	comment
VCSEL	-5 dBm	-3 dBm	specified to manufacturer
100 m multimode fibre	0.5 dB	0.3 dB	specified by FOnetworks[33]
3 MTP-MTP interfaces	1.5 dB	0.6 dB	taken from [35]
power at receiver	-7.0 dBm	-3.9 dBm	
receiver sensitivity	-16 dBm	-18 dBm	specified in [28]
power margin	9.0 dB	14.1 dB	

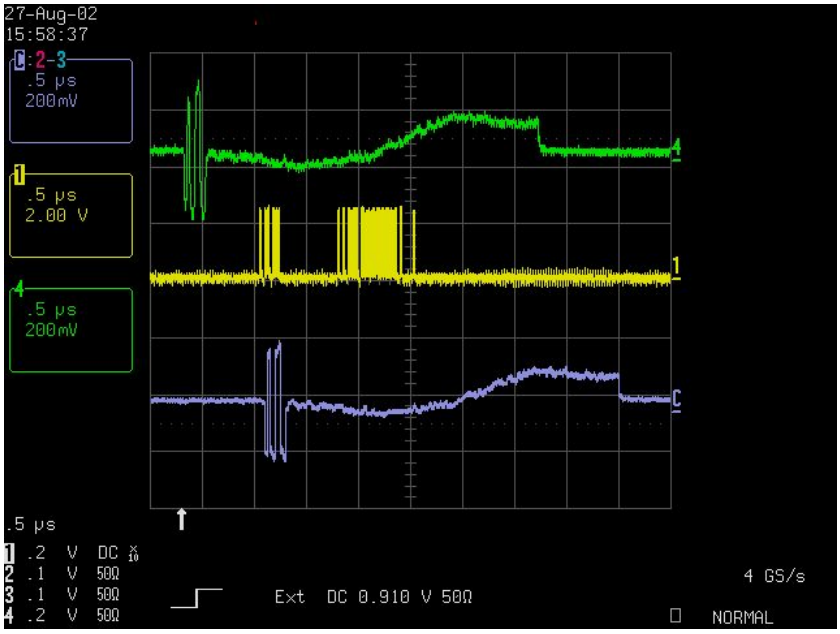

Figure 7.10: First transmitted baseline of a Beetle 1.1 The upper trace is the analogue signal before transmission, the middle trace one of the 8 bits after digitization and the lower trace the reconstructed signal after transmission.

Chapter 8

Radiation Qualification

In this chapter, the hazard of radiation induced effects and related components failures is described. Due to the proximity of the Silicon Tracker to the beampipe and the interaction point, the readout electronics are subjected to high fluences of ionizing particles and radiation. As all active electronic devices with exception of the radiation-hard Beetle chip are located in the Service Box, this chapter only discussed the radiation qualification for Service Box components. The location of the Service Boxes were chosen such that for 10 years of nominal LHCb operation, the estimated total ionizing dose levels are below 15 krad and the fluence of neutrons with an energy equivalent of 1 MeV is below $2 \cdot 10^{12}$ n/cm^2 [36].

Radiation induced effects may temporarily or permanently affect or inhibit normal operation. After a short overview of the effects, which can be triggered the radiation in our proposed readout system, all components in question are listed, evaluated and their sensitivity to radiation is characterized.

8.1 Radiation Induced Effects in Electronic Devices

Radiation induced effects in electronic devices can be categorized into three classes:

- single event effects (SEE)
- displacement damage
- total ionizing dose (TID) effects

This section describes all three effects with special emphasis on their influence on the Silicon Tracker readout system.

The first group of effects result from single interactions of highly ionizing particles in silicon. By depositing enough charge inside an electronic circuit, its functionality can be disturbed or it can even be destroyed.

- Single Event Upset (SEU): If a digital signal, stored in a memory cell, is upset by an energetic particle, this is called a single event upset or SEU. Although it is mostly seen in memory circuits like static or dynamic RAM circuits, logic signals themselves can also be toggled by an SEU. The SEU is particularly dangerous for configuration memories, where program code for programmable devices is stored. Different to SEUs in logic data circuits, where an SEU will fake a signal, a changed program code bit persists until reprogrammed. In the worst case, this might lead to the complete loss of the functionality of the device. Introducing redundancy into the design of digital circuits, the sensitivity to SEU drastically decreased. Although it does not prevent the generation of an SEU, the effects on the following electronics are greatly suppressed by implementing triple redundancy with majority voting elements or error detection and correction circuits (EDAC) with parity bits to locate and correct errors.

- Single Event Latchup (SEL): Single event latchup is the radiation induced version of the standard latchup failure mechanism of CMOS devices. Parasitic bipolar transistors created by alternating p- and n-doped regions in the silicon bulk can be triggered and then short circuit the supply voltage to ground. While standard latchup is prevented by a proper circuit layout, radiation induced latchup can still lead to the disabling or destruction of a device. If the current through the short-circuit is small, a power-cycle may clear the latchup and restore normal operation. If the current density is too high, the circuit will be damaged permanently. ASIC designers can prevent SEL by applying special design rules. For users of COTS devices however, the only way to ensure that a device is not sensitive to SEL is its characterization by radiation testing.

- Single Event Burnout (SEB): Single event burnouts are mainly seen in power MOSFET transistors of power supply circuits. Via regenerative feedback in the device, the drain current increases up to burnout of the source-drain channel. No such device is used in the Silicon Tracker.

The second class of radiation induced effects is displacement damage caused by hadrons that displace atoms in the silicon lattice. For bipolar transistors, this results in a gain loss as the vacancies and interstitial atoms in the lattice enhance the recombination current in the base. For optical devices like pindiodes and laserdiodes, the displacement damage leads to intermediate states in the semiconductor bandgap, which may influence the performance of the device. CMOS devices are generally not affected by displacement damage. The general method used to characterize the displacement damage is by neutron irradiation, with the irradiation fluence being normalized to the equivalent of the effects induced by neutrons of 1 MeV energy. The normalization is done via the Non Ionizing Loss Equivalent (NIEL) scaling [37]. Experience shows, that the displacement damage is independent of whether the device is powered or not, so most neutron irradiations are performed with unpowered devices.

The third class of radiation damage is due to total ionizing dose effects (TID). In MOS structures, ionizing radiation deposits charge inside the isolating gate oxides (*trapped charges*). This charge generates an electric field which shifts the gate threshold voltage of the field-effect transistor. Additional TID effects are increased noise and leakage currents or an increased number of interface states. However, it has been shown that smaller scale CMOS processes are

less sensitive to buildup of trapped charge in the gate oxide, as the smaller oxide thickness (less than 10 nm) allows a faster tunneling of the charge out of the gate oxide. A further mechanism to increase the TID tolerance of a device is the use of enclosed transistors to prevent leakage currents between devices on the bulk. If these design rules are implemented, mixed-signal devices capable of withstanding doses of 10 Mrad and more are possible. Bipolar components also suffer from TID damage, although to a much lesser degree. For COTS components, a first selection of components can be done by choosing small scale CMOS processes, preferrably deep submicron. Even without special radiation tolerant design, this process scale provides some inherent immunity against TID effects.

Proton irradiation is particularly interesting for device testing, as all three damage mechanisms (SEE, displacement damage and TID) are covered with a single irradiation campaign. A 50 MeV proton fluence of 10^{11} p/cm^2 is equivalent to a TID of 14 krad and a NIEL of $1.8 \cdot 10^{11}$ n/cm^2 with an energy equivalent of 1 MeV [38].

A more detailed discussion of radiation induced failures of semiconductor devices can be found in [39].

8.2 Overview of Potentially Radiation Sensitive Components

This section takes a closer look on the used devices, where radiation damage might occur.

- The AD8129 line receiver from Analog Devices Inc. is a bipolar device, which is manufactured in a proprietary bipolar process. The parameters in question after irradiation are gain, bandwidth and supply current. The tests are performed after separate neutron and proton irradiations.

- The TSA0801 8 bit analogue-to-digital converter is a deep-submicron CMOS device produced by ST microelectronics [24]. Being a mixed-signal device (analogue and digital), the testing of the ADC is more challenging, as both parts of the device have to be characterized. Possible TID effects are loss of gain, increased non-linearity and increased noise. Also, some internal digital circuitry can be knocked out by high radiation doses, leading to missing digital output codes and resulting in harmonic contents in the digitized data. SEU effects would be upsets of digital bits (converting '0' into '1' and vice versa) or latchup of digital outputs. As CMOS devices are not sensitive to neutron irradiation, the ADC testing was restricted to proton irradiation.

- The 850 nm VCSEL is the optical transmitter, which converts the electrical signal into a light signal. As displacement damage may play a key role in the performance of an optical device, the VCSEL diodes can be irradiated with neutrons and protons. Unfortunately, the choice to use the ULM-Photonics VCSEL diode was taken after the neutron campaign period, so only a proton irradiation was done for this VCSEL, while the neutron irradiation wa performed with the VCSEL from Honeywell. However, due

to NIEL scaling, a 60 MeV proton fluence can also be normalized to the equivalent of 1 MeV neutrons. Using a conversion factor of 1.8 means 10^{11} p/cm^2 are in this case equivalent to $1.8 \cdot 10^{11}$ n/cm^2.

- For the optical fibre, the main defects will be radiation induced color centers, which will increase light scattering and therefore light attenuation. Therefore, the fibre is irradiated with neutrons and protons. While the cable used for the neutron fluence irradiation has a core diameter of 62.5 μm, the proton irradiation campaign included a 62.5 μm sample and a fibre with a core diameter of 50 μm, identical to the version foreseen to be used in the experiment. According to the manufacturer, the material used for fibre production is the same. Hence, it allowed us to compare the proton induced damage of the two cable types with each other.

8.3 Description of Test Setups and Results

The neutron irradiation is relatively simple, as the devices under test do not have to be powered during the test. It is therefore sufficient to document the performance of the test samples before the irradiation campaign and compare this to the results obtained after the neutron exposure. The irradiation was performed in April 2003 at the Prospero reactor at CEA Valduc, France. The devices under test and the associated neutron fluences are listed in Table 8.1.

Table 8.1: Neutron irradiated components and associated fluence levels.

Component	units irradiated	1 MeV eq. neutron fluence [n/cm^2]	multiple of 10 LHC years
AD8129	5	10^{13}	5
line receiver	5	$2 \cdot 10^{14}$	100
HFE4390-541 VCSEL	1	$7 \cdot 10^{13}$	35
optical cable	8 m	10^{13}	>5
10 μF ceramic	5	10^{13}	5
capacitors	5	$2 \cdot 10^{14}$	100

The listed VCSEL type from Honeywell has no relation to the later used Ulm-Photonics VCSEL. It was included in the test as it was the only VCSEL available at the time of the neutron irradiation campaign. The 10 μF ceramic capacitors were included to study possible effects of neutron fluence on a standard passive component, although this type of component is widely believed to be insensitive to the levels of radiation encountered in typical high energy physics experiments.

The irradiation of components with protons was performed in two separate campaigns between November 2003 and February 2004 at the Proton Irradiation Facility PIF at PSI, Switzerland. The proton energy was 60 MeV with a particle flux of $4 \cdot 10^8$ p/(cm^{2}sec). This flux corresponds to a dose rate of approximately 60 rad/s. The achieved doses for the individual components are listed in Table 8.2.

Table 8.2: TID tested components and associated radiation levels.

Component	units	TID[krad]	multiple of 10 LHC years
AD8129 line receiver	4	300	20
ULM-Photonics VCSEL	3	300	20
optical cable	1 cable (12 fibres),60 mm	2200	ca. 150
TSA0801 ADC	4	60	4
ADC10040 ADC	4	60	4

8.3.1 Line Receiver

For the operation amplifiers the gain was measured for frequencies between 0.1 and 500 MHz. The gain vs. frequency was measured using a network analyzer, that was set to a start frequency of 0.1 Mhz and a stop frequency of 500 MHz. The analyzer sweeps with a sinewave source through the programmed frequency range and records the received power for all frequencies. Such a measurement takes typically less than one second and is therefore very easy to perform. Care has to be taken, however, regarding the matching of input and output of the amplifier. Standard network analyzers are designed for 50 Ω impedances and return irregular results for a mismatched device-under-test. The input matching was implemented with a simple 50 Ω resistor to ground, while the output matching could only be achieved by using a series resistor, increasing the load of the amplifier output into its operating range. A series resistor of 1000 Ω was chosen together with a 50 Ω resistor to ground. A schematic of the matching is shown in Figure 8.1.

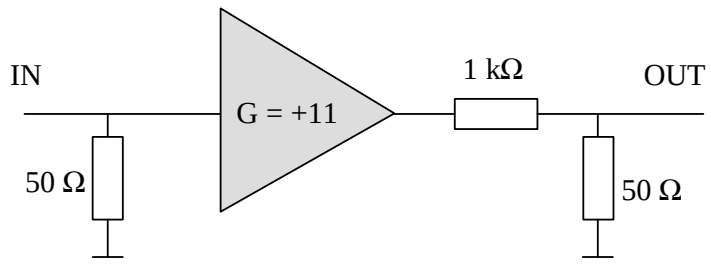

Figure 8.1: Simplified schematic of the line receiver matching to 50 Ω.

While this provides a 50 Ω load to the analyzer input, it also acts as a voltage divider. Taking into account the internal 50 Ω termination of the input, one obtains:

$$\frac{50||50}{50||50+1000} = 0.0244 = -32.26 \text{ dB}$$

If the voltage amplification of the amplifier is now added, :

$$\text{Gain G} = 1 + \frac{2200}{220} = 11 = 20.83 \text{ dB}$$

then the total gain is -11.43 dB. However, this is specific to this test setup, as a result of the need to match to the low impedance network analyzer and is not related to the application circuit of the Silicon Tracker readout. For a injected signal power of -20 dBm (which corresponds to 22 mV at 50 Ω), an output level of -20 dBm + $(-11.43$ dB$) = -31.43$ dBm is thus expected.

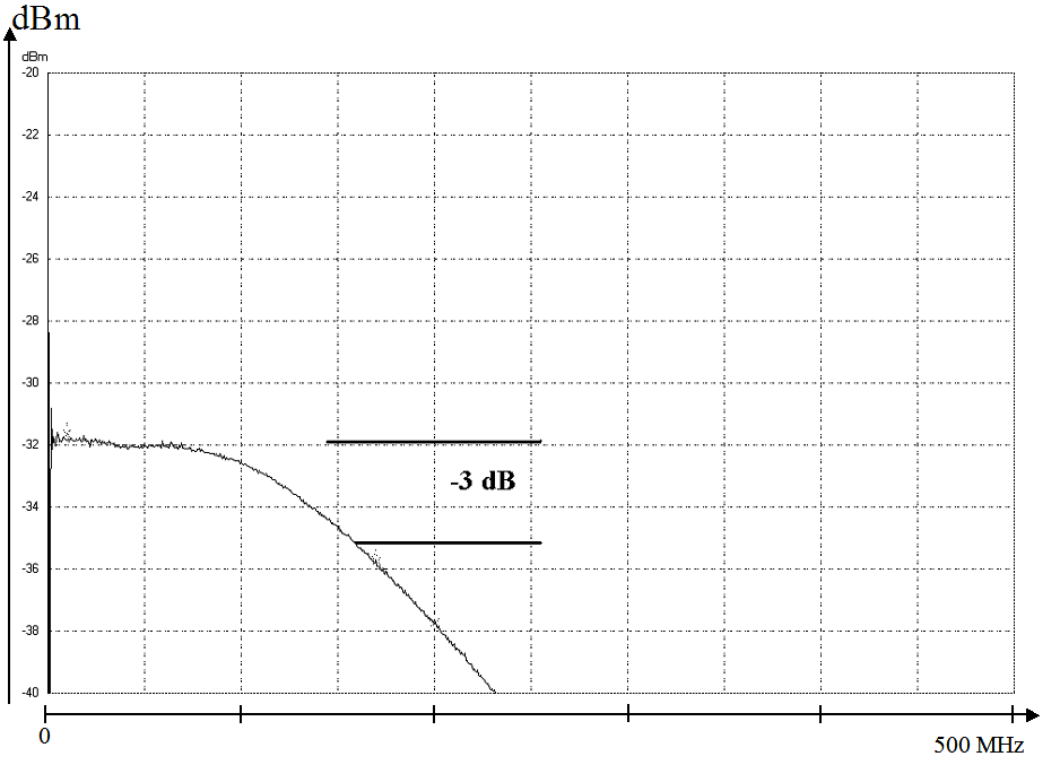

Figure 8.2: AD8129 gain plot before irradiation.

As an example, Figure 8.2 shows the frequency response of an unirradiated amplifier. The flat top at -31.4 dBm is easily seen with the roll-off towards higher frequencies beginning at around 100 MHz. The bandwidth is quoted as the frequency, at which the gain has dropped to 3 dB below the low frequency gain. In our case, the measured bandwidth is around 170 MHz, in perfect agreement with the datasheet. The performance of the amplifiers was characterized by comparing pre- and post-irradiation gain, bandwidth and supply current.

Results Four line receivers were characterized before irradiation and after cummulative TID doses of 10, 30, 50, 70, 100, 150 and 300 krad. A slight increase in gain of 0.2 dB was observed for all samples, which gradually built up during the irradiation. When converted into linear scale, the 0.2 dB gain difference translates into a voltage gain increase of 2.3 %,

which is considered to be negligible for the Silicon Tracker application. The bandwidth of the line receivers gradually decreased from initially 170 MHz to 150 MHz, as seen in Figure 8.3. This should not affect the overall performance, especially when taking into account that the tested dose of 300 krad is one order of magnitude above the expected dose in the experiment. The current consumption was monitored for the sum of all four devices. It stayed constant at 40 mA, in compliance with the datasheet [22].

For the ten devices, that were exposed to neutron fluences of up to $2 \cdot 10^{14}$ n/cm^2, the gain variation and bandwidth after irradiation were characterized in the same way. For the five samples that were exposed to a fluence of 10^{13} n/cm^2, no gain or bandwidth variation could be observed. Moreover, no change in the supply current was seen. For the five samples with the higher neutron fluence, the gain showed a slight increase around a frequency 70 MHz and a reduced bandwidth of about 150 MHz (see Figure 8.3). In addition, the supply current decreased by 10 %. As for the proton irradiated samples, these minor changes in device performance are not considered to have an effect on the operation in the experiment.

8.3.2 VCSEL Diodes

The neutron irradiation testing of the Honeywell VCSEL diode was done by comparing the output power as a function of the laser diode current before and after irradiation. As the VCSEL was already mounted on a GOL prototype board, the GOL internal laser driver was used to generate the laser currents. For the proton irradiation testing of the ULM-Photonics VCSEL, only the power output for a given current was measured directly before and after irradiation.

Results As the Honeywell VCSEL, which was included in the neutron test is not the same device, that will be used in the experiment, this result can not be regarded as a radiation qualification for LHCb. It is quoted here for completeness. The radiation qualification for the ULM-Photonics VCSEL was performed with proton irradiation only and the induced displacement damage was normalized to an 1 MeV-equivalent neutron fluence.

The Honeywell VCSEL diode experienced a power loss of about 0.6 dB after a neutron fluence of $7 \cdot 10^{13}$ n/cm^2. The power loss is clearly visible in Figure 8.4, in which the output power is shown as a function of the GOL bias current setting. The 'knee' at about 27 mA is caused by the lower binary state of the GOL data entering the laser mode and contributing to the average power that is measured by the optical power meter. It is therefore an indication of the laser threshold current. As the position of this 'knee' did not change after irradiation, we conclude that the laser threshold was not affected by the neutron irradiation. Two origins of the power loss are possible: radiation induced darkening of the ball lens that is used to focus the laser light emitted from the VCSEL into the fibre, or a decrease of the VCSEL power output itself.

For the ULM-Photonics VCSEL diodes that were included in the proton irradiation test, a constant current source was used to supply the diodes with a DC-current without any

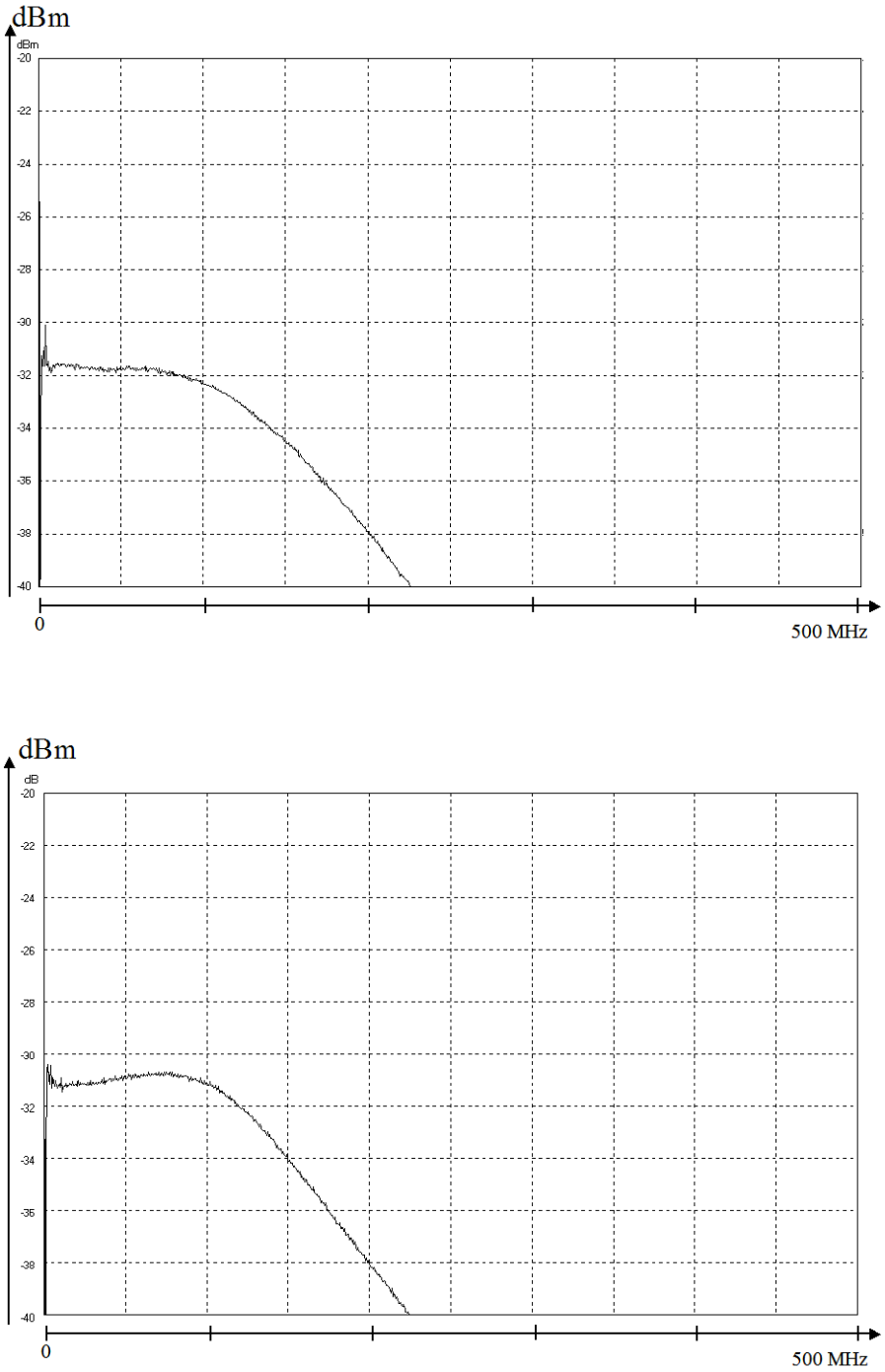

Figure 8.3: AD8129 gain plots after a TID of 300 krad (top) and a after neutron fluence of $2 \cdot 10^{14}$ n/cm^2 (bottom).

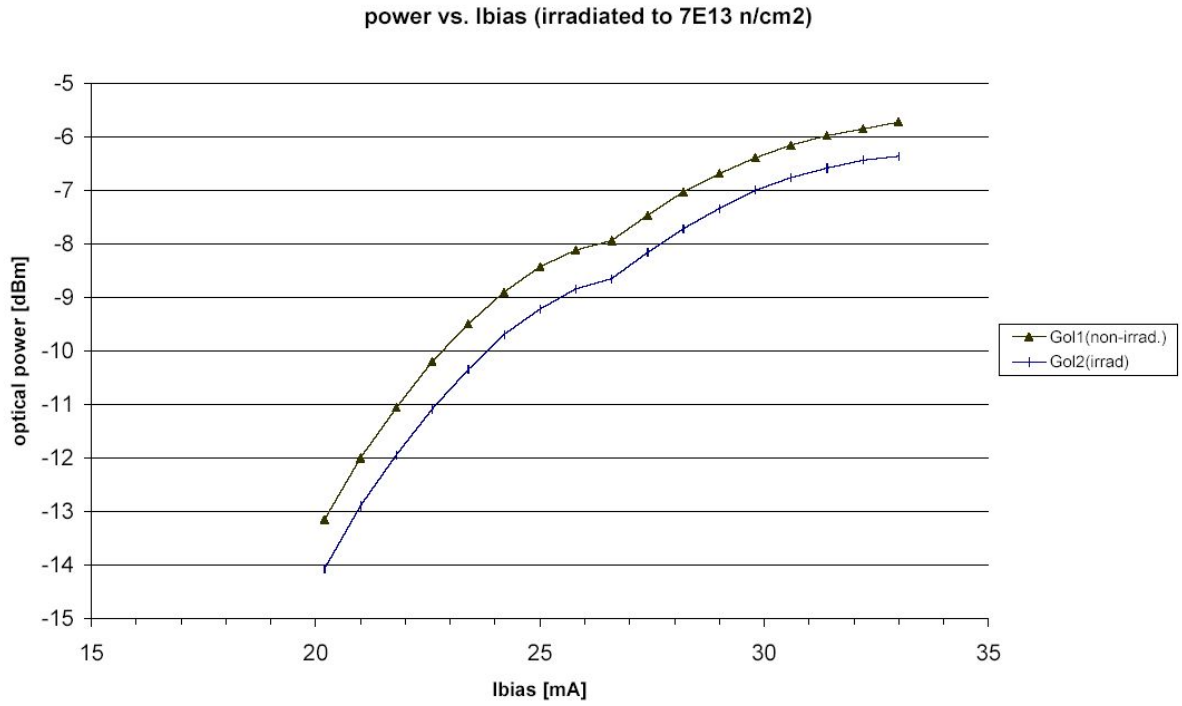

Figure 8.4: Mean optical power of the Honeywell VCSEL vs. GOL bias current setting after a neutron irradiation of $7 \cdot 10^{13}$ n/cm^2.

modulation. The power output of the VCSEL was measured before and after the irradiation. After a TID of 300 krad, which is equivalent to a 1 MeV neutron fluence of $3.6 \cdot 10^{12}$ n/cm^2, no power loss could be observed within the precision of the measurement, which is approximately 0.3 dB.

8.3.3 Optical Cable

To determine the induced attenuation of the optical cable, the attenuation before and after irradiation was measured using a 850 nm light source and an optical power meter, both produced by Sys-Concept Inc. [40].

Results The fibre sample that was exposed to a neutron fluence of 10^{13}n/cm^2 was simply checked by comparing post-irradiation attenuation to pre-irradiation values.

Figure 8.5 shows the absolute attenuation of each of the single fibres in an 8 m long sample of 12-fibre ribbon cable. For each point, the reproducability of the fibre mating accounts to a measurement uncertainty of about 0.3 dB. Within the precision of the measurement, no indication for neutron fluence induced attenuation could be observed. The fibre is therefore considered not to suffer from the neutron fluences encountered in the LHCb environment.

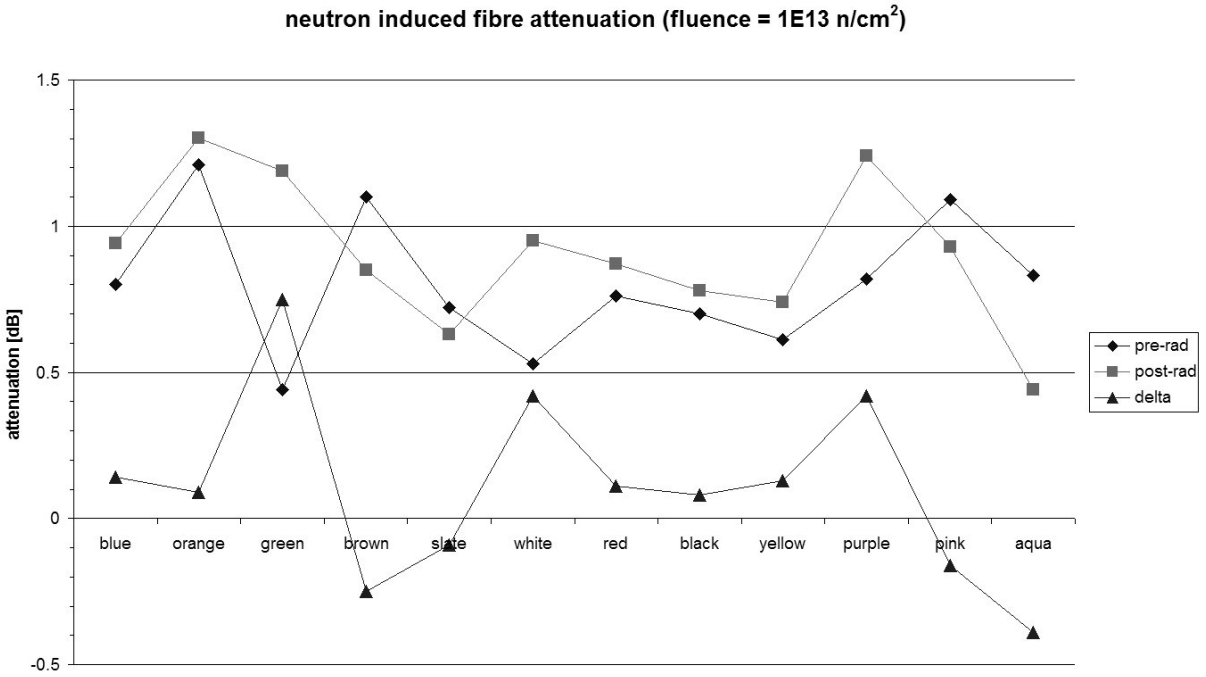

Figure 8.5: Optical attenuation of the twelve tested fibres before and after irradiation with a a neutron fluence of 10^{13} n/cm^2. The third set of points shows the difference of the measurements before and after irradiation.

For the proton irradiation of the 62.5 μm fibre, 3 of the 12 fibres in the breakout part of the cable were routed across the illuminated spot, which resulted in an irradiated length of 90 mm per fibre. As the far end of the fibre was located outside of the irradiation bunker, a real-time measurement during irradiation was possible. For the irradiation of the 50 μm fibre in the second campaign, the ribbon part was routed twice across the beam spot. To normalize the obtained measurements to the first test, the obtained attenuation values were multiplied by 0.5. As the beam spot size was reduced to 60 mm diameter after an integrated dose of 270 krad during the second campaign, the normalization factor was changed accordingly to 0.75 to report the effective fibre attenuation for a length of 90 mm.

As shown in Figure 8.7, a continuous increase of the attenuation was observed up to a TID of 1000 krad, corresponding to a 1 MeV equivalent neutron fluence of $1.2 \cdot 10^{13}$ n/cm^2. At this point, the corresponding attenuation was about 9.5 dB for 90 mm of irradiated length. Continued irradiation did not result in increased attenuation, suggesting a saturation effect, which was not further investigated.

The fibres in the LHCb experiment will start at the Service Boxes and go through the shielding wall to the counting house. At the detector side of the shielding wall, but not close to the detector, the TID level for 10 years of operation is expected to be of the order of 500 rad [36]. For an estimated length of 50 m of fibre in the radiation area, this can be integrated to 25 krad $\cdot$ m. To account for the section of the cable close to the detector, which is expected

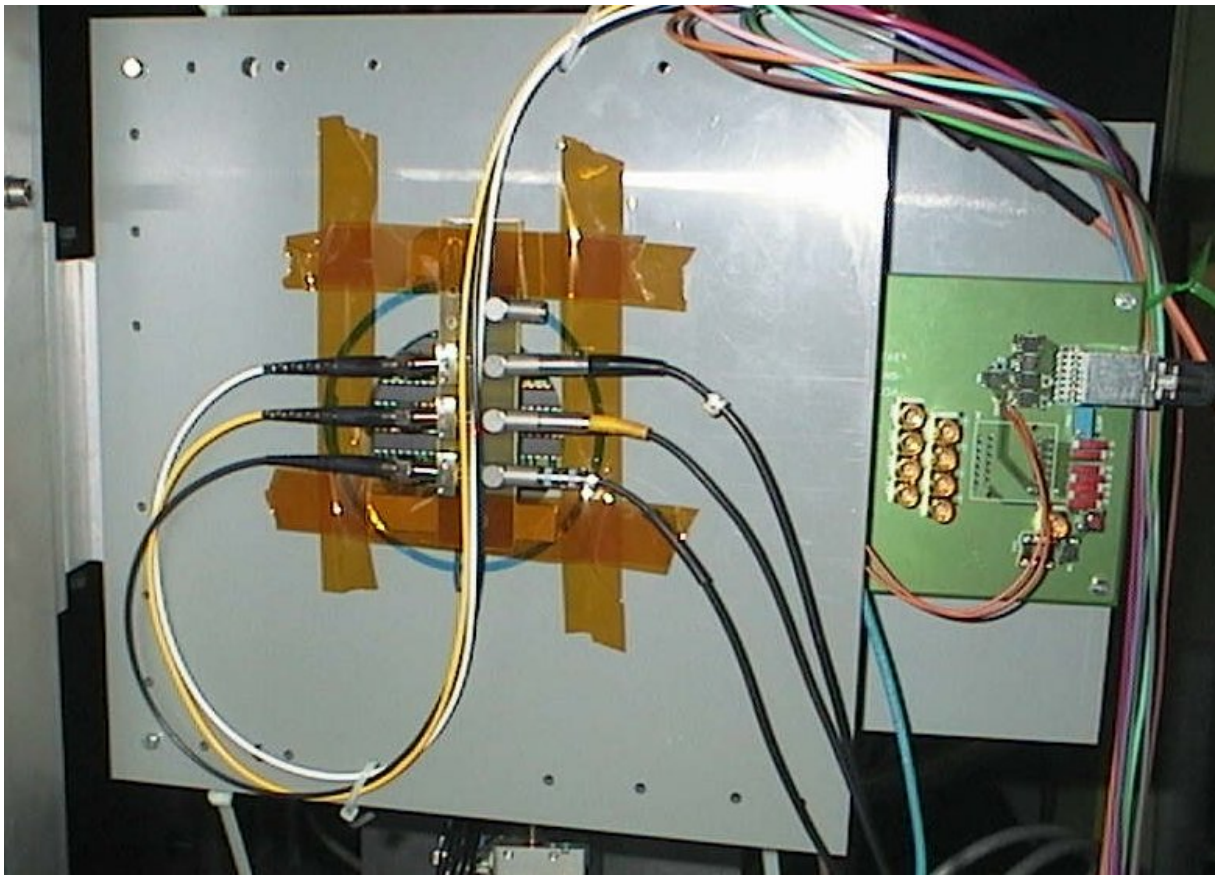

Figure 8.6: Test setup for the proton irradiation of the fibre and the VCSEL diodes.

to experience up to 15 krad over 10 years, another 25 krad · m are added, to give a total integrated dose of 50 krad · m. When scaled to a length of 90 mm, this is equivalent to a dose of approximately 550 krad. As the actual dose on the fibre in the experiment is in the order of 10 krad, a linear extrapolation is performed on the irradiation data to ignore nonlinear effects in the attenuation for high doses. This extrapolation is indicated in Figure 8.7 and leads to a expected loss of about 10 dB.

This loss is of the order of the power margin of the optical transmission system calculated in Section 7.6, which was already assumed as worst case scenario. As the radiation damage of optical cables will mainly occur in the first meters of each fibre due to their close distance from the beampipe, a replacement of this cable section can to a large extent compensate for the radiation induced attenuation. This replacement is made possible by having a patch panel at a distance of about 10 m from the detector (see Chapter 12).

8.3.4 Fast ADCs

Two fast ADCs produced by different companies were included in the radiation qualification: the TSA0801 from ST microelectronics [24] and the ADC10040 from National Semiconductor

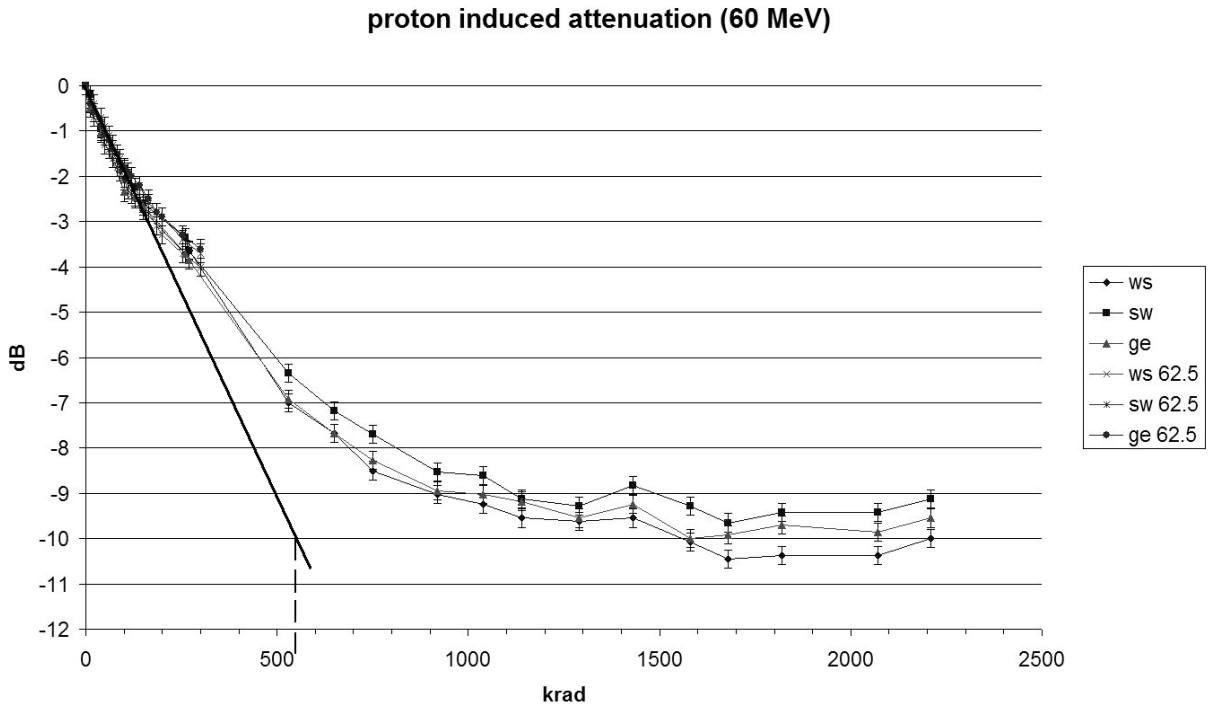

Figure 8.7: Proton induced optical fibre attenuation for three fibres each with 50 and 62.5 μm core diameter and an normalized to an irradiated fibre length of 90 mm. An extrapolation to apply this data for low doses and long cable lengths has been added.

[41]. While the TSA0801 is entirely fabricated in 0.25 μm CMOS, the ADC10040 has CMOS process scales of 0.18 μm for the core logic and 0.4 μm for the output drivers.

As both ADCs are CMOS devices, they were not irradiated with neutrons but with protons only. During the proton irradiation, both ADC's were tested for TID effects and single event effects. Concerning TID effects, a combined measurement was performed to determine linearity, gain, noise and missing digitizer codes. This was done by digitizing a 5 MHz sine wave with an amplitude close to the fullscale of the ADC. To reduce the harmonic components of the source signal, the 5 MHz sine generator was followed by a 5^{th} order lowpass filter. As the test setup only supported two devices at once, multiple irradiation runs had to be performed after each other. Two ADCs per run were connected to an ACEX FPGA PCI-board [42], which stored 2048 samples per device in a FIFO memory for subsequent readout and analysis by MATLAB. This readout was done once every 5 seconds during irradiation, which is sufficient for TID damage determination.

The relevant properties are Signal-to-Noise ratio (SNR) and Spurious-free Dynamic Range (SFDR). As both parameters are best characterized in the frequency domain, the first operation performed on each data packet of 2048 samples was a discrete Fourier transformation (DFT). A basic assumption of the discrete Fourier transformation is the periodicity of the incoming data packet. By definition, the discrete Fourier transformation of a finite number of samples results in the same output as a Fourier transformation of an infinite multiple of

such a single data packet, when concatenated one after another. However, discontinuities in general occur at the borders between two consecutive packets as illustrated in Figure 8.8.

These discontinuities generate fake frequency components in the Fourier transformed data. This can be prevented by multiplying the single data packet with a so-called 'window function'. By applying such a function to the data, the data samples close to the edges of the packets are less weighted than the center samples, therefore suppressing discontinuities between packets. For our application, the Blackman window function was chosen, which is parameterized as:

$$f(i) = 0.42 + 0.5 \cdot cos(i \cdot \tfrac{\pi}{m}) + 0.08 \cdot cos(2i \cdot \tfrac{\pi}{m})$$

with $m = 1024$ and i ranging from -1024 to +1023. The Blackman window function is also shown in the middle of Figure 8.8. The weighted sine-wave packets are shown at the bottom of Figure 8.8. The difference between a DFT without window function compared to a DFT with the Blackman window function is shown in Figure 8.9. A more detailed discussion of window functions can be found in [43].

The same procedure is dapplied to determine SNR and SFDR for commercial devices. The values and graphs obtained in our measurements can therefore be compared directly to data given in the datasheets of the devices.

SNR The Signal-to-Noise Ratio (SNR) can be used to measure the gain and noise of the ADC. The SNR is calculated by integrating the signal power of the 5 MHz test signal and dividing it by the noise power integrated up to the Nyquist bandwidth limit of 20 MHz, which is half the sampling rate of the ADC. The result is usually expressed in dB for easy comparison with the specified SNR of the device.

SFDR The linearity of the ADC can be affected by radiation, either by direct influence of the analog gain stages before digitization or by damage in the digital logic section, e.g. stuck bits. Both effects result in a distortion of the input signal, which in the case of this test is a sinewave. According to Fourier's theorem, such a periodic distortion will lead to an increase of harmonic components, also called spurious signals, which can be directly observed in the Fourier-transformed data. The effect is usually expressed by the Spurious-Free Dynamic Range or SFDR, the amplitude ratio between the main signal and the largest spurious signal, given in dBc[1]. As any ADC will have an inherent non-linearity, this parameter is quoted in the datasheet. However, a direct comparison between specified values and those obtained during the irradiation tests is difficult, as imperfect grounding and shielding of the setup can degrade the results. Still, a comparison of the data taken before, during and after the irradiation is possible and was therefore performed.

[1] dBc: dB relative to main carrier

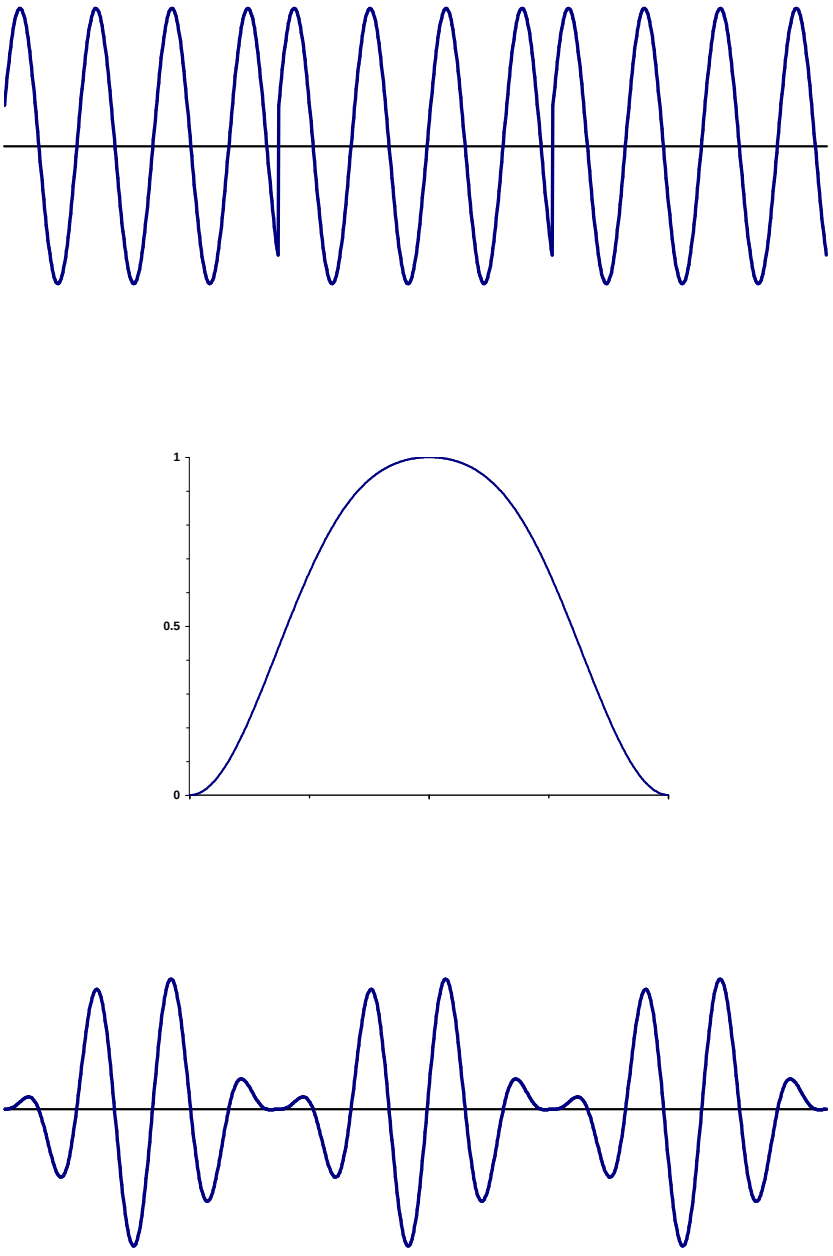

Figure 8.8: Three packets of a recorded sine-wave concatenated after each other (top), showing discontinuities at the packet borders. The middle plot is the Blackman window function for a single packet. The bottom plot shows the product of the raw data with the Blackman window function for three consecutive packets.

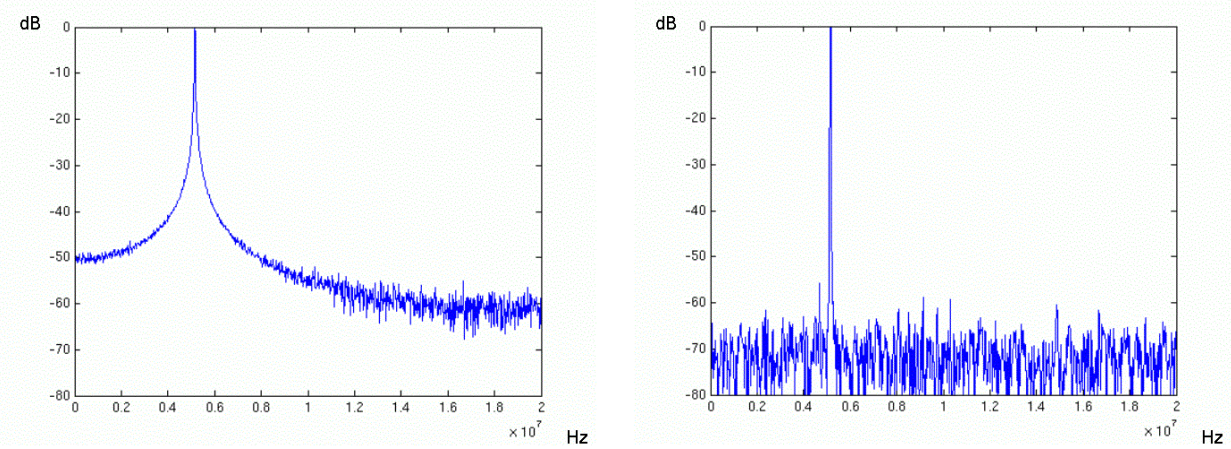

Figure 8.9: DFT data without window function (left) and with Blackman-Window function applied (right). In both cases, the spectral power from -80 to 0 dB is plotted here vs. the frequency in the range between 0 and 20 MHz.

SEE Testing The TID setup was not suitable for SEE testing of the logic part of the ADC, as data was not taken continuously. Since single event effects may only last one clock cycle, their detection requires continuous monitoring. To simplify the measurement, it was performed using standard logic gates, which required the digital output to have a defined state. This was achieved by connecting the ADC inputs either to their high limit, resulting in all output bits being '1', or connecting the inputs to ground, which lead to all output bits being '0'. As the probability for a logic signal flipping from '1' to '0' state might not be identical to the probability of a '0' state being flipped to '1', both cases had to be monitored. The outputs were compared via clocked logic gates, which served as an input for a counter, increasing its value by one for each clock cycle in which an 8-bit word differed from the expected pattern. Any stuck output bit caused by a single event latch-up would lead to the counter incrementing with every clock edge, which would be observable as well.

Results For each of the two ADC types, four devices were included in the TID test and another four in the SEE test. As each test setup could monitor only two devices at once, the samples were divided into two batches which were tested after each other. For the TID test devices, the measured SNR and SFDR were plotted in Figures 8.10 and 8.11, as a function of total ionizing dose. For none of the 8 devices any radiation related TID effect was observed. During the irradiation of the first batch of samples of the ADC10040, a sharp decrease of signal amplitude by 30 % was observed after a dose of 5 krad. As this happened in both devices simultaneosly, the effect was quickly traced back to the signal source. The failure was assumed to have its origin either in the LEMO cabling to the test setup or to the LEMO termination resistor, which was unintentionally placed in the beam spot as well. After exchanging the cabling and the termination resistor, the full signal amplitude was restored for the second batch of the ADC10040.

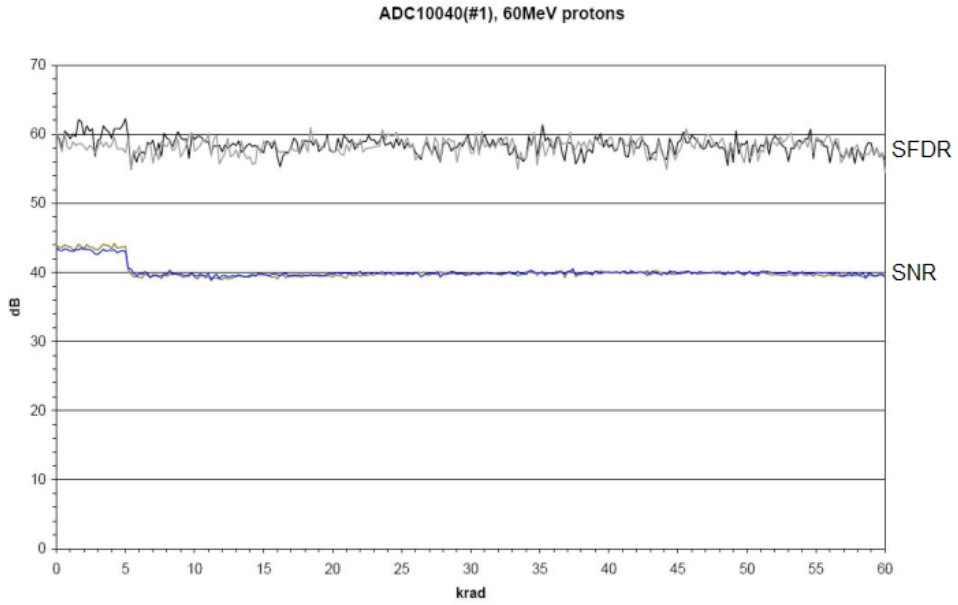

Figure 8.10: SNR and SFDR vs. TID for one the two ADC10040 batches. The spectral power in dBc is plotted vs. the received dose.

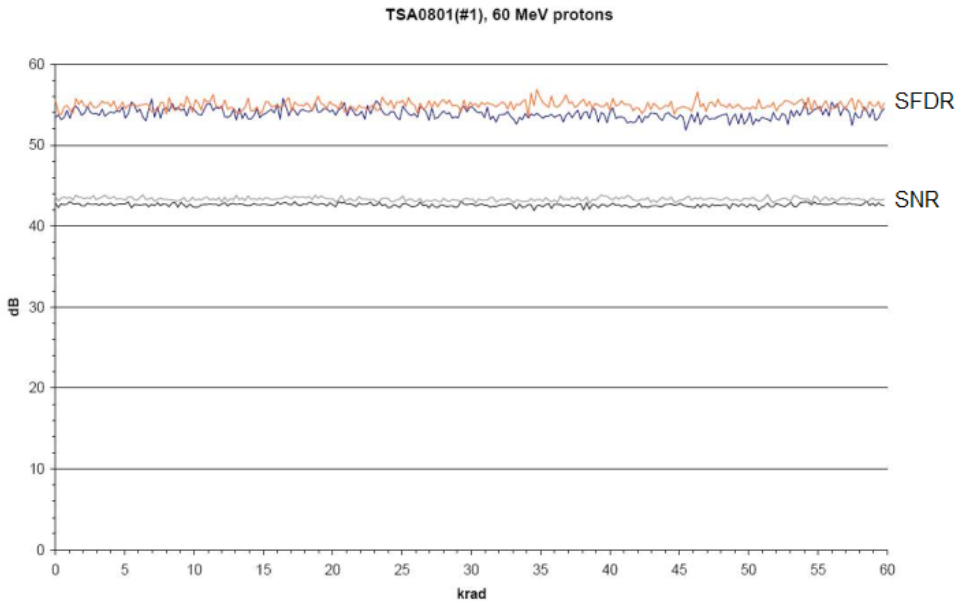

Figure 8.11: SNR and SFDR vs. TID for one of the two TSA0801 batches. The spectral power in dBc is plotted vs. the received dose.

The SEE testing resulted in one single bit flip from '1' to '0' in one of the TSA0801 devices. No SEE was observed in the ADC10040 devices. Extrapolated to the complete number of 8512 devices used in the LHCb Silicon Tracker, this would lead to 2128 SEUs in the Silicon Tracker for a total proton fluence of $4 \cdot 10^{11}$ p/cm^2, which was the fluence applied during testing. This is approximately a factor of 4 more than expected in the Service Box environment for 10 years of LHCb operation. This SEU rate is considered to be low enough to have no significant effect.

To estimate the effect of latched bits in the TID testing, a sample data file recorded in the lab was taken and deliberately modified such, that various bits from the 8-bit output word were individually set to zero before processing them. The resulting plots for setting no bit, bit 0, bit 1 and bit 2 to zero are shown in Figures 8.12. Again, the spectral power in dBc is plotted vs. the frequency in Hz. An increased noise for each manipulated bit can be seen, with higher noise for more significant bits. In addition, the introduced nonlinearity caused a significantly increased amount of spurious signals, which could be easily detected by the SFDR measurement.

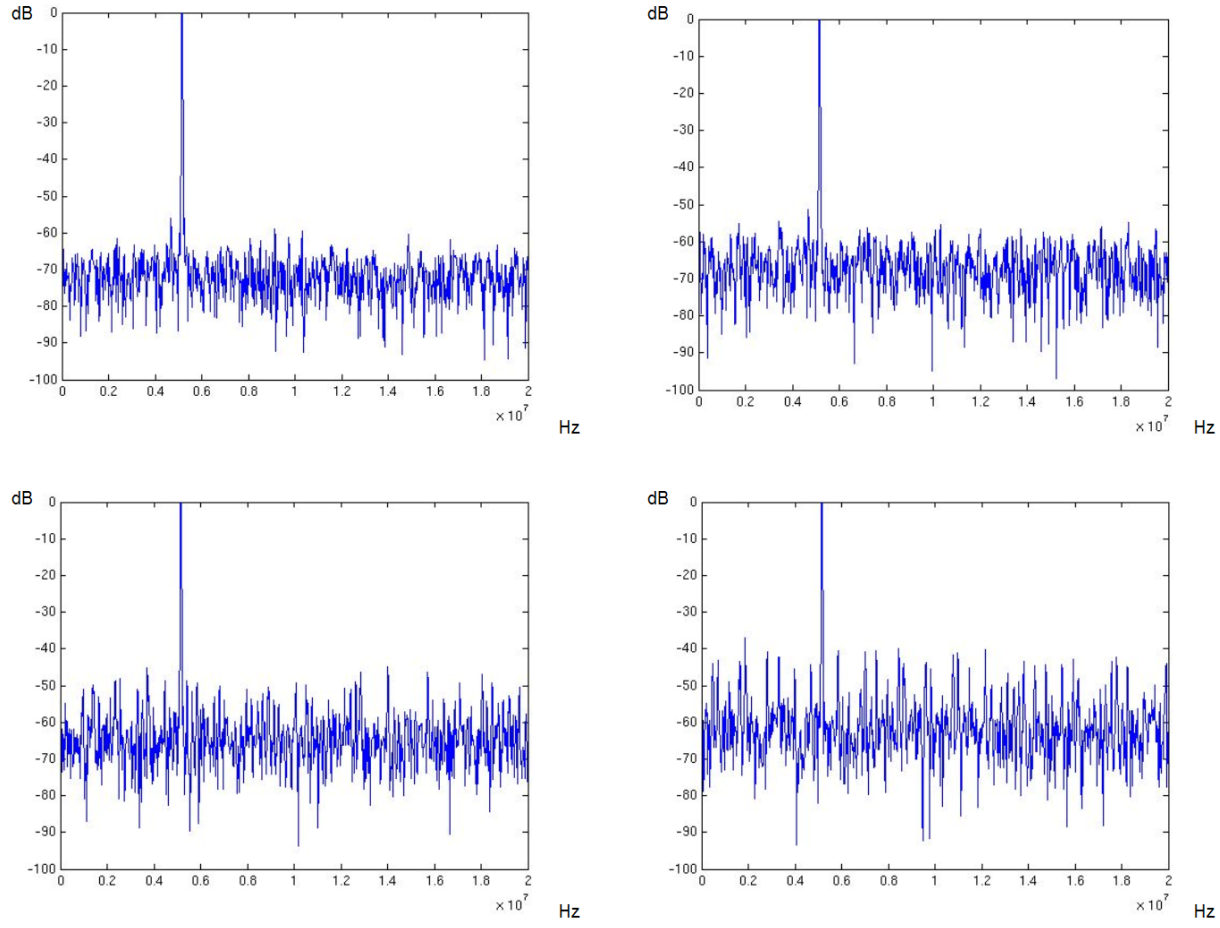

Figure 8.12: Original DFT data (top left) and bit 0 (top right), bit 1 (bottom left) and bit 2 (bottom right) set to zero.

Chapter 9

Connectivity to LHCb TFC + ECS Systems

The LHCb Silicon Tracker has to be integrated into the LHCb timing and fast control network and the LHCb experiment control system. In this section, the basic specifications of these two systems and their interfaces to the LHCb Silicon Tracker are described.

9.1 The LHCb Timing and Fast Control Network

The LHCb Timing and Fast Control (TFC) network provides those signals to the LHCb detector where exact timing is needed. These are the clock and trigger signals but also reset signals and calibration signals. The distribution of these signals throughout the experiment is done using Timing, Trigger and Control (TTC) system hardware common to all LHC experiments. Additional LHCb specific hardware like the Readout supervisor (RS) or the TFC switch is specialized to handle the high Level-0 decision rate of about 1 MHz. A general scheme of the LHCb TFC network is shown in Figure 9.1.

The Readout Supervisor multiplexes the global LHC clock with fast signals generated locally at the LHCb experiment, such as Level-0 and Level-1 trigger signals, reset signals and calibration signals. The multiplexed signal is distributed via optical fibres to the detector subsystems, where the optical signal is received and the fast signals are extracted from the serialized data stream. In this section, only the component with direct connection to the LHCb Silicon Tracker is described in detail, which is the TTCrx decoder chip. For a more detailed description of the LHCb TFC system, see [45]. The global TTC system used by all LHC experiments is described in [47].

The TTCrx decoder chip has been developed by the CERN microelectronics group and is produced in a radiation-hard 0.8 μm DMILL technology [46]. It demultiplexes the TTC datastream, which is received by a photodiode and converted to electrical data. Internal registers of the chip can be accessed via the optical data stream or a standard I2C interface. Of

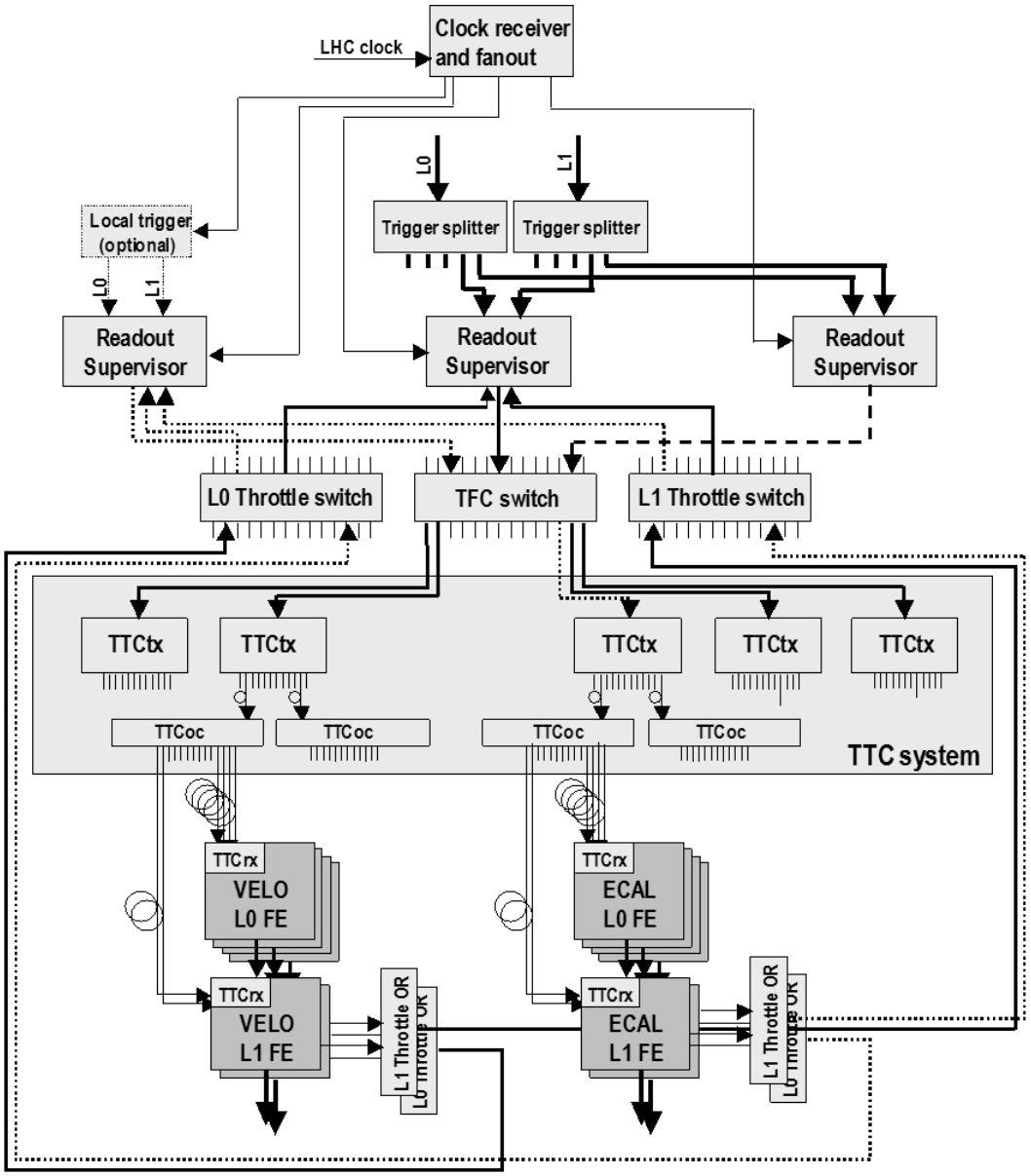

Figure 9.1: Overview of the TFC architechture (from [45]).

particular interest for the LHCb Silicon Tracker are the following signals, which are provided by the TTCrx:

- Broadcast command signals
- general LHC clock (40.079 MHz)
- Level-0 accept signal[1]

[1]In the TTC network description, the LHCb Level-0 accept signal is referred to as the L1accept signal. This is because LHCb is the only experiment with a trigger level 0.

A simplified block diagram of the TTCrx is shown in Figure 9.2.

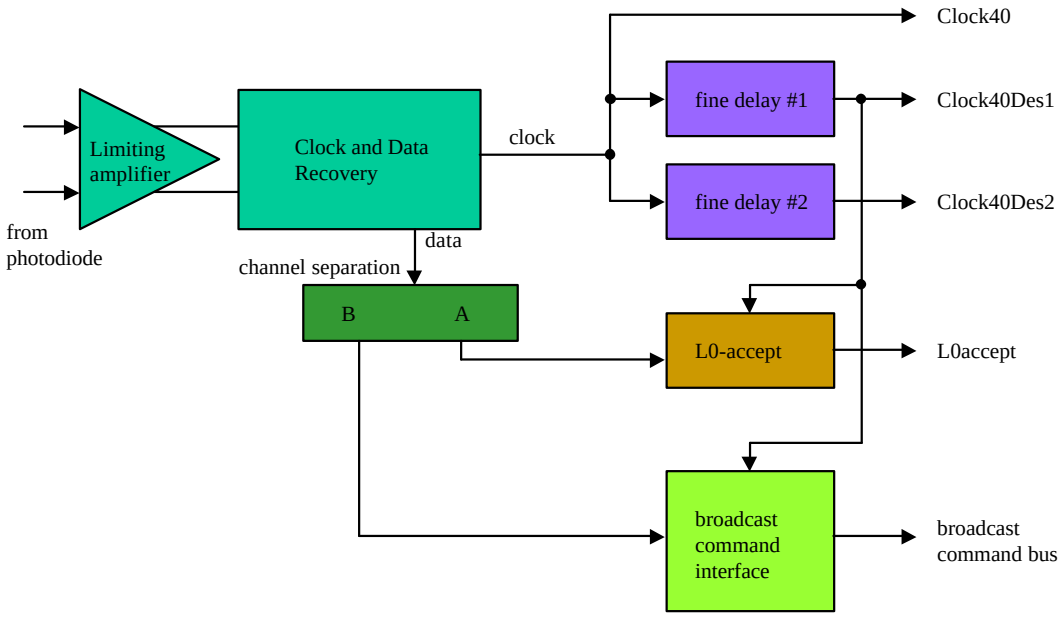

Figure 9.2: Simplified blockdiagram of the TTCrx decoder chip. Only the sections with relevance for the Silicon Tracker are shown.

The TTC broadcast commands are inserted into the TFC network by the Readout Supervisor. Two broadcast command formats are used in LHCb. A short broadcast command distributes the Level-1 trigger decision, reset and calibration signals. Bunch counter and event counter reset signals are distributed in addition, but are not used by the Silicon Tracker frontend electronics. The long broadcast command is used to distribute the IP address of the assigned CPU node for the Level-1 trigger and the HLT (see also [45]).

An additional decoder is needed to generate the reset and calibration signals, which are distributed via short broadcast commands. This decoding is performed in the main FPGA on the SPECS slave mezzanine (see Section 9.2). The Level-1 trigger decision is not required by the Silicon Tracker frontend electronics and can be therefore neglected.

The TTCrx provides the LHC clock on three different outputs: straight from the clock recovery circuit (Clock40) and via two internal delay lines, which allow the generation of two clock outputs (Clock40Des1, Clock40Des2) with independently adjustable phase delays. Each delay line allows to adjust the timing of its clock in steps of 104 ps.

The broadcast command signals and as a consequence the reset and calibration signals, are synchronized to the Clock40Des1 signal. This signal also provides the clock for the Beetle

chips, so that the reset signal will arrive at the Beetle with a fixed phase relation. The same would be true for the calibration signal. However, its phase relation has to be adjustable with respect to the Beetle clock to perform timing scans of the frontend electronics. This is accomplished by using the delay25 clock delay chip on the Control Card (see Section 10.2).

The Clock40Des2 output is used to provide the ADCs and the GOL serializers with a clock. As the Clock40Des2 output can be independently shifted with respect to the Clock40Des1 output, the timing relation between the Beetle and the ADCs can be adjusted to optimize the sampling point of the ADCs on the Beetle data. After this optimization has taken place, Clock40Des1 and Clock40Des2 can be shifted together to optimize the timing of the readout with respect to the particle passage through the detector.

The hardware unit that is is used for the Silicon Tracker frontend electronics is the TTCrq mezzanine. It features a TTCrx fitted to a photodiode on a plug-in module. In addition, the TTCrq is also equipped with a QPLL chip [48]. The development of the QPLL low-noise PLL was necessary, as the jitter of the clock which was delivered by the TTCrx was determined have a too large jitter for high speed operation of the GOL serializer. By filtering the TTCrx clock with the QPLL, a low-jitter clock can be supplied to the GOL.

9.2 The LHCb Experiment Control System

The LHCb Experiment Control System (ECS), provides the user with control and monitoring access to the detector systems. The ECS allows the user to change and read back settings of the detector frontend and to reprogram FPGAs without physically accessing the hardware. In addition, environmental parameters like voltages, currents and temperatures, which are critical for the detector operation are also read out via the ECS system.

The ECS software is provided by the LHCb ECS group and is based on a common graphical user interface. In this way, easy interaction between different software modules working within the LHCb system can be ensured. Different hardware units are supported by the common ECS system. The system chosen by the Silicon Tracker is the SPECS, which is developed by the LHCb calorimeter group of LAL Orsay [49]. It consists of two parts: the SPECS master, shown in Figure 9.3, and the SPECS slave mezzanine, shown in Figure 9.4. The SPECS master is located in the counting house while the SPECS slave will be integrated into the on-detector electronics, close to the frontend readouts. The two units are connected to each other via standard networking cable[2]. The data transmission uses a proprietary bus protocol with a data rate of 10 Mbit/s.

The SPECS master is a PCI card that can be plugged into a standard PC. It can directly connect to up to four SPECS slave mezzanine cards. The SPECS slave mezzanine is based on a radiation tolerant antifuse FPGA from Actel Inc. [50]. It provides up to eight I2C buses or eight JTAG buses, and 32 generic input-output pins that can be individually configured.

[2]An optical interconnection was considered but eventually rejected due to the lack of radiation qualified optical components.

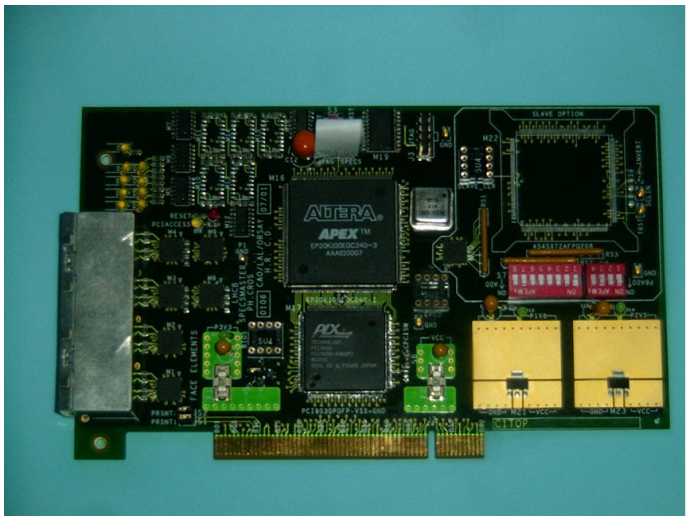

Figure 9.3: The SPECS PCI master board.

Figure 9.4: The SPECS slave mezzanine.

Furthermore, the SPECS slave mezzanine includes a radiation tolerant slow-control ADC to read out environmental parameters. Another feature is a decoder for the short broadcast commands of the TTC system. When connected to the TTCrx broadcast command bus, the SPECS slave mezzanine can be used to generate the Level-0 reset signal and the calibration signal. Multiple SPECS slave mezzanines can be connected together locally and share a single connection to a SPECS master. This reduces the number of required SPECS master cards for a given number of SPECS slaves.

Chapter 10

Design and Performance of the Service Box

The Service Box provides all necessary electrical signals and connections to the detector. The elements of the Service Box are designed as modular components to simplify development, production, commissioning and maintenance. A main objective in the design of the Service Box was reliability and robustness, concerning not only operation but also production. Where possible, all parts were designed with sufficiently large margins to compensate for any component variations.

A general overview of the Service Box and its connections is shown in Figure 10.1. Each readout hybrid is connected to one Digitizer Board. Up to 16 Digitizer Boards per Service Box are mated to a common backplane, which distributes power, fast timing signals and slow control to the Digitizer Boards and to the readout hybrids. These signals are generated in a single Control Card per Service Box. Voltage regulators for supplying the readout hybrids and the Service Box itself with power are located on the backplane.

The different components of the Service Box are discussed in the following subsections.

10.1 Digitizer Board Design

The Digitizer Board is the main element inside a Service Box. In order to achieve a 1:1 association between readout hybrids in the Silicon Tracker and Digitizer Boards, the Digitizer Board not only receives and processes the analogue data coming from its associated readout hybrid, but it also provides fast timing signals, slow control signals and power. The main functionality of the Digitizer Board is the processing of the data produced by a readout hybrid. The remaining signals and the power are merely passed on from the Control Card via the backplane and Digitizer board to the interface to the readout hybrid, the Digitizer Board input connector.

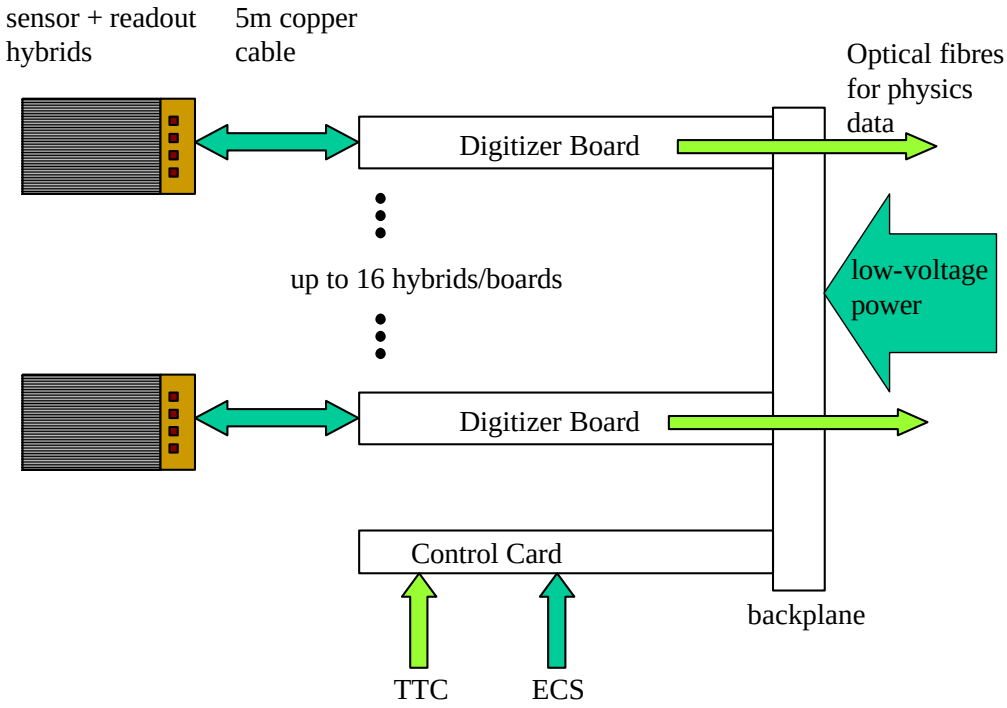

Figure 10.1: Schematic overview of the Service Box components and their connections to the detector.

The Digitizer Board is produced in a multilayer technology with impedance controlled traces. The heights of the individual layers are shown in Figure 10.2. The thicknesses were chosen to provide controlled impedance traces for the layers *Signal2* and *Bottom* when produced from FR-4 material with an average dielectric constant of 4.5.

Figure 10.3 shows the layout of the Digitizer Board. The interface to the readout hybrid is seen on the left, where the 5 m long SCSI copper cable is connected. The connector on the rightis the interface to the Service Box backplane, providing power and timing and control signals for the Digitizer Board and its associated readout hybrid.

Figure 10.4 shows the channel assignment of a TT Digitizer Board. As a TT hybrid features four Beetle readout chips, 16 analogue channels have to be digitized. The Digitizer Board for the Inner Tracker will be similar to the TT Digitizer Board, but digitizes only 12 analogue channels. Four circuits blocks are used to process the data from the four Beetles. Each block uses four line receivers with four ADCs, one GOL and one VCSEL. The link synchronization circuit is located at the top left, while a QPLL clock clean-up circuit and a slow-control ADC are located on the bottom right. In the center of the board, the root of the clock distribution tree can be seen.

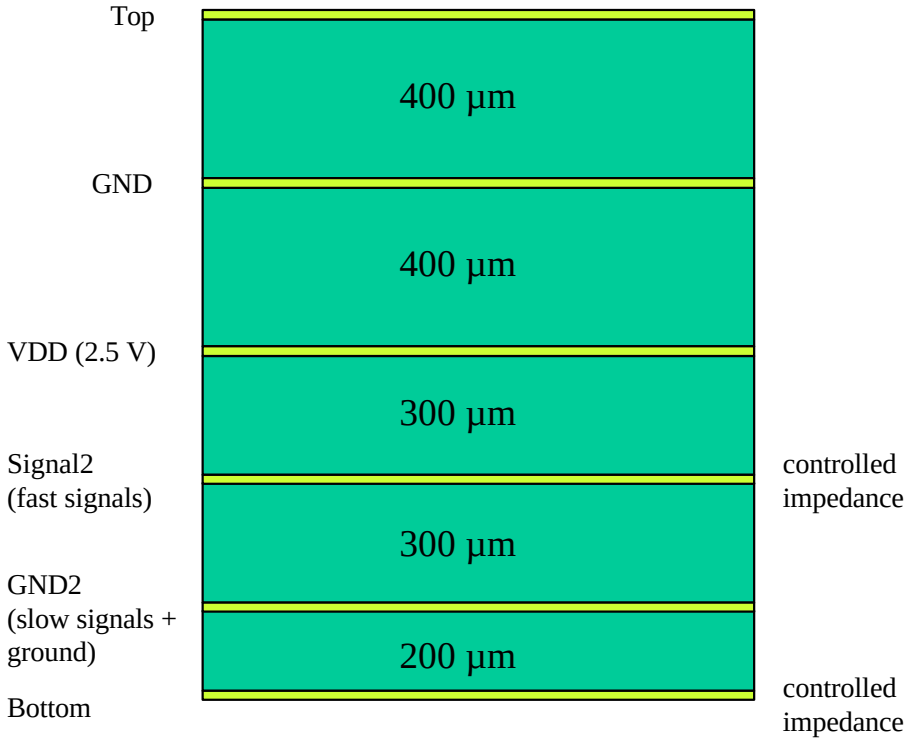

Figure 10.2: Height of the layers in the Digitizer Board.

Figure 10.5 shows a pre-series Digitizer Board during testing. In the following sections, the basic building blocks on the Digitizer Board are discussed.

10.1.1 Detector Data Processing and Transmission

The data from a readout hybrid enters the digitizer board via 12 differential signal pairs for a Inner Tracker readout hybrid or 16 signal pairs for a Trigger Tracker hybrid, corresponding to three and four Beetle chips per hybrid, respectively. This analogue data is received and amplified before digitization. The basic elements of a single analogue input stage are shown in Figure 10.6. The digital data is further processed in the GOL serializer, which encodes the data and drives a VCSEL diode connected to optical fibre. A simplified schematic diagram for the digital part is shown in Figure 10.7.

For each differential signal, the AD8129 amplifier matches the signal amplitude to the input of the ADC and converts the signal to a single-sided signal ready for digitization. The optimal gain of 10, which is proposed in the datasheet has been shown to be too large for use with the Beetle 1.3, as this version has an enhanced output driver when compared to its predecessor, the Beetle 1.2. A differential voltage divider is included at the input of the

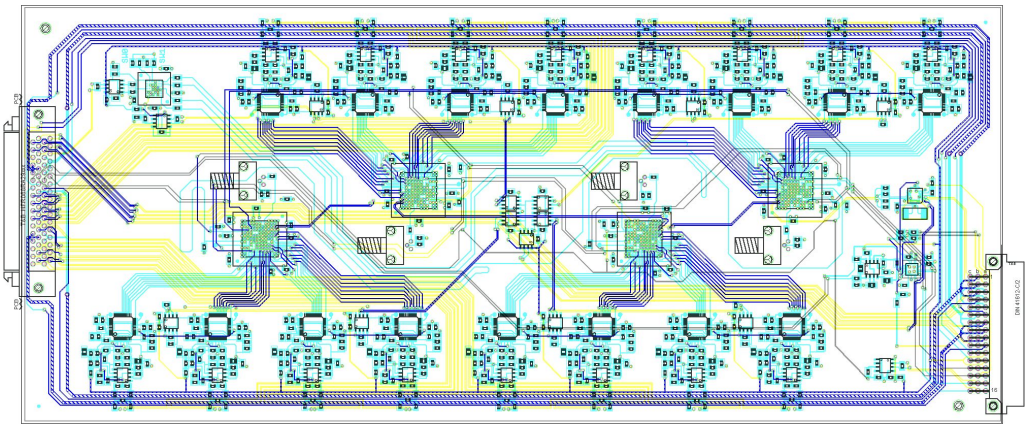

Figure 10.3: Layout of the Digitizer Board.

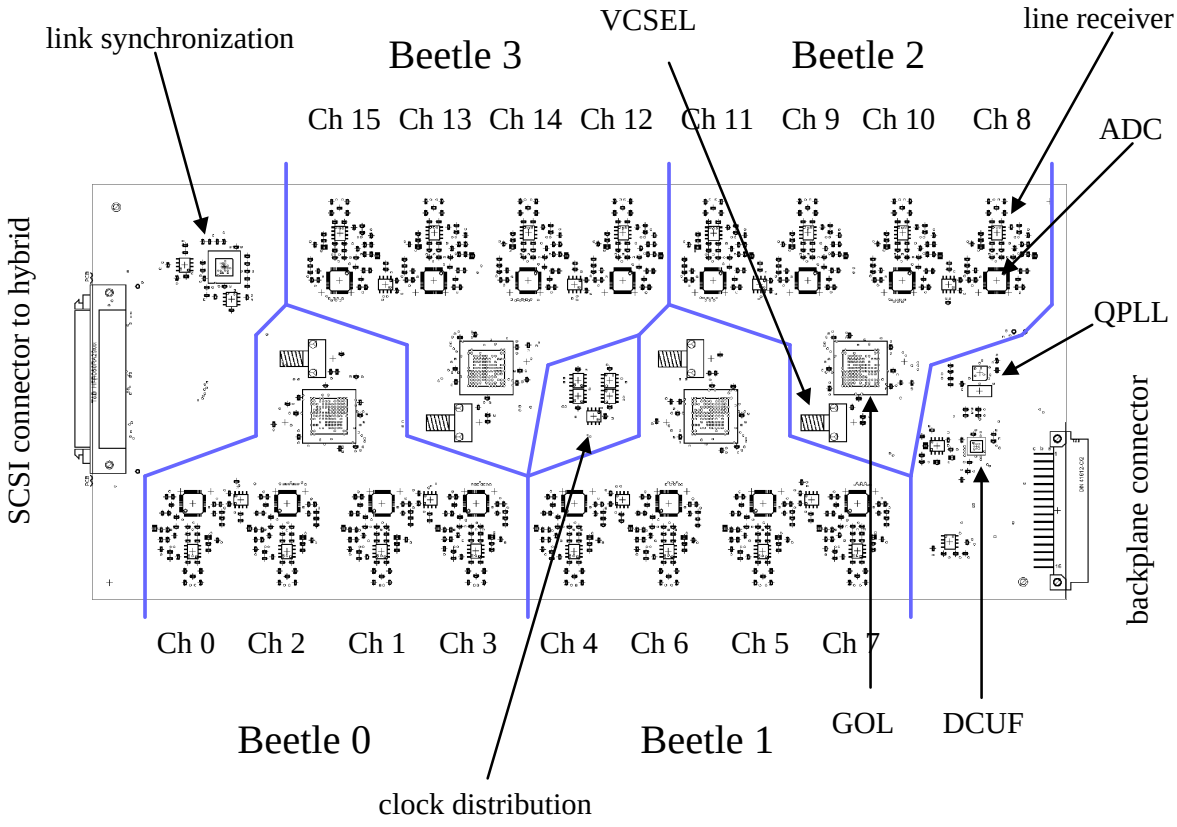

Figure 10.4: Beetle channel assignment on the Digitizer Board.

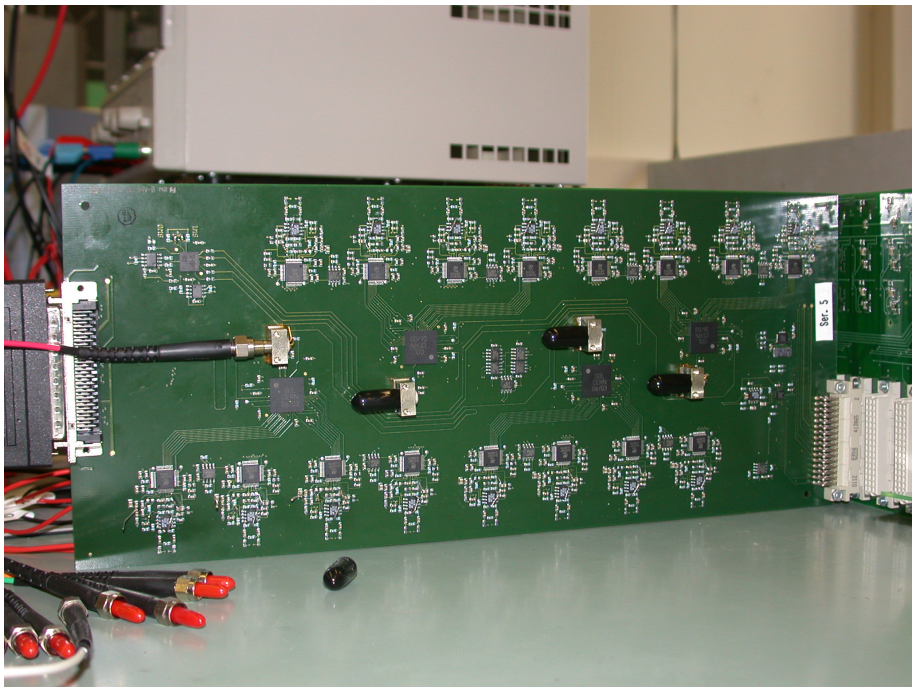

Figure 10.5: The Digitizer Board during testing.

amplifier reducing the total gain to about 2.4.

The actual dynamic range of the complete system was determined by using the internal testpulse of the Beetle. The load capacitance at the load capacitance was here 0 pF, as all input pads of the Beetle hybrid, that was used for this tests, were completely unbonded. The resulting plot is shown in Figure 10.8.

Saturation is reached for positive charge signals equivalent to 140000 e^- and for negative signals equivalent to 129000 e^-. It was verified by probing the *OutOfRange* pin of the ADCthat the limiting device is the ADC, which is driven in saturation.

The measured dynamic range covers well the linear range of $\pm$ 110000 e^- of the Beetle chip for zero load capacitance. Together with the gain reduction of the Beetle for large load capacitances, which was discussed in Section 5.2.2, this gain setting is considered to be appropriate for use in the Silicon Tracker.

The input bandwidth of the Digitizer Board is determined by the input lowpass and the bandwidth of the amplifier itself. The conversion of the time constant of the lowpass gives 1.6 kHz for the low limit and 170 MHz as a high limit from the datasheet of the line receiver. This is considered to be sufficient for conditioning the Beetle analogue signal before digitization.

With both the ADC and the CERN Gigabit Optical Link serializer (GOL) using CMOS logic levels for the digital signals, the interconnection of these devices can be done without any additional circuitry. By placing the ADCs and the GOL as close as possible to each other,

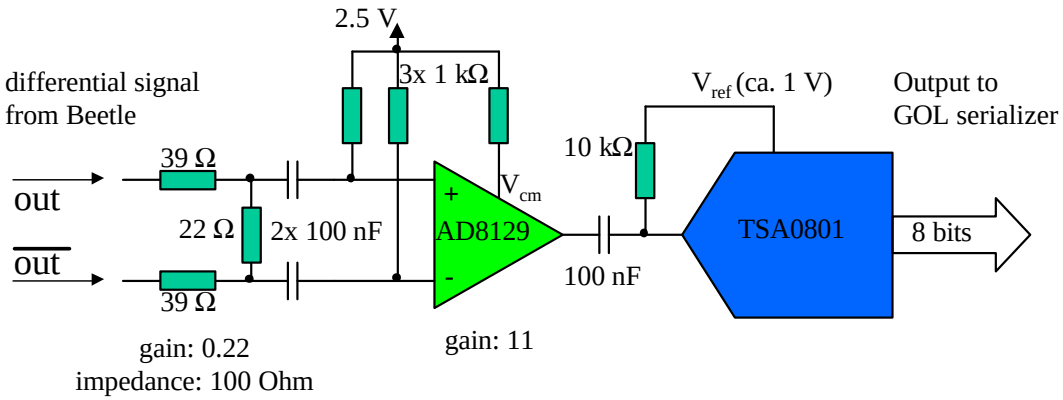

Figure 10.6: Block diagram of a single analogue input stage of the Digitizer Board. 16 of these stages are used in parallel for a TT Digitizer Board, 12 for an IT Digitizer Board.

a maximum trace length of less than 60 mm could be achieved. For transmission lines of an electrical length of under $\lambda/10$, where λ is the wavelength of the highest transmitted signal component, connections are considered as being electrically short and impedance matching can be omitted. For our 60 mm long traces, this translates into a wavelength limit of 600 mm, which when combined with an average dielectric constant of $\epsilon = 4.5$ for standard FR-4 board material results in a frequency of approximately 235 MHz. As the signals in question are digital signals with a minimum duration of 25 nsec, the fundamental frequency component is 20 MHz. As a result, no impedance matching between ADC and GOL is required. The shortest connection is about 30 mm long, resulting in a maximum trace length difference of 30 mm. When translated into signal time skew, 30 mm correspond to 0.2 nsec, so all digital signals between ADC and GOL are in phase within 0.2 nsec. This is considered to be sufficient for reliable operation of the interconnection.

The GOL serializer provides different operational modes, some of them programmable via I2C or JTAG, others to be determined by connecting special pins to either ground or VDD. The GOL default settings implemented on the digitizer board are listed in Table 10.1.

As the JTAG protocol is not used in the Silicon Tracker, the JTAG interface of the GOL is connected such that it does not interfere with I2C commanding of the GOL device. This is achieved by hardwiring notJTAGRST to GND and JTAGTCK, JTAGTDI, JTAGTMS to VDD.

While some of the hardwired parameters are completely fixed by this, other values, for example the PLL charge pump current and the mean laserdiode current, can be reprogrammed via the I2C interface. For these parameters, the hardwired value represents the power-up default, which is set before any user intervention.

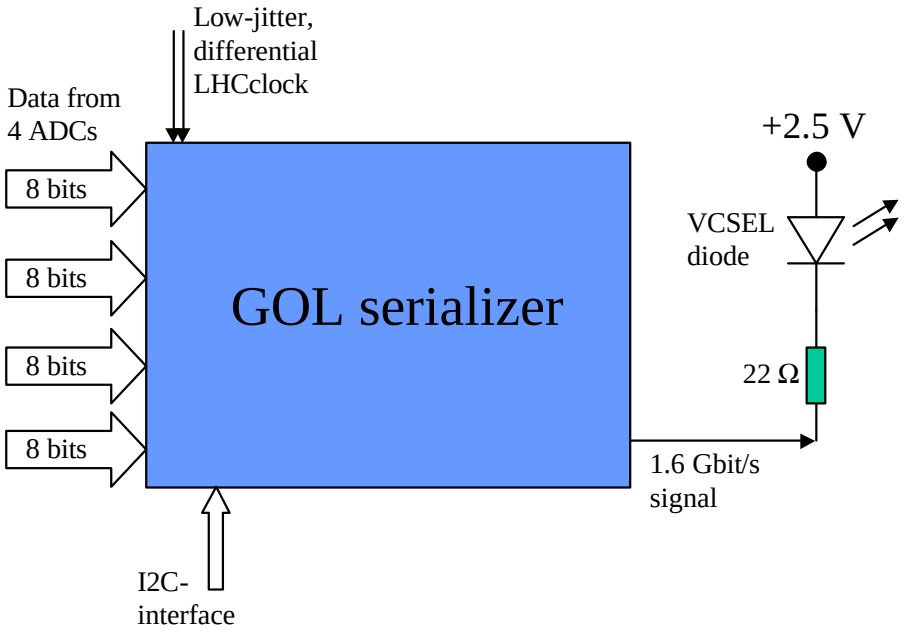

Figure 10.7: Simplified schematic diagram for the digital data processing.

The GOL chip provides a *conf_negedge* pin which permits to select the active clock edge according to the timing relation of the clock compared to the data at the GOL device. This pin had to be connected to GND. If it had been connected to VDD, the GOL would have latched the data and control signals to the falling edge, however only within a very narrow allowed time window. The use of this mode was thus discouraged by CERN microelectronics group [21]. Instead, it was proposed to swap the LVDS signal lines of the clock coming arriving at the GOL. This solution is implemented in the design of the Digitizer Board. The decision which polarity of the clock to use, has only to be done once during prototyping, as the setup and hold times of the GOL inputs are 5 ns and 3 ns, respectively. When compared to the duration of 25 ns of a digital input signal, this leaves a window of 17 ns that is allowed for the positive clock edge with respect to the data edge. If one polarity would be determined to place the clock edge within the bad time region of 8 ns width, a swap of the clock lines would shift the edges relation by 12.5 ns, well into the allowed timing region.

Figures 10.9 and 10.10 show the location of the rising edge of the clock with respect to the data lines going into the GOL. As no differential probe was available, the positive LVDS signal was monitored using a standard probe, hence the low signal quality. To check for the timing differences between the four ADCs connected to a group, a short connection of about 30 mm was compared to a long connection of about 60 mm using a GHz-Bandwidth, low capacitance probe. As predicted, the signal skew between these signals was barely visible

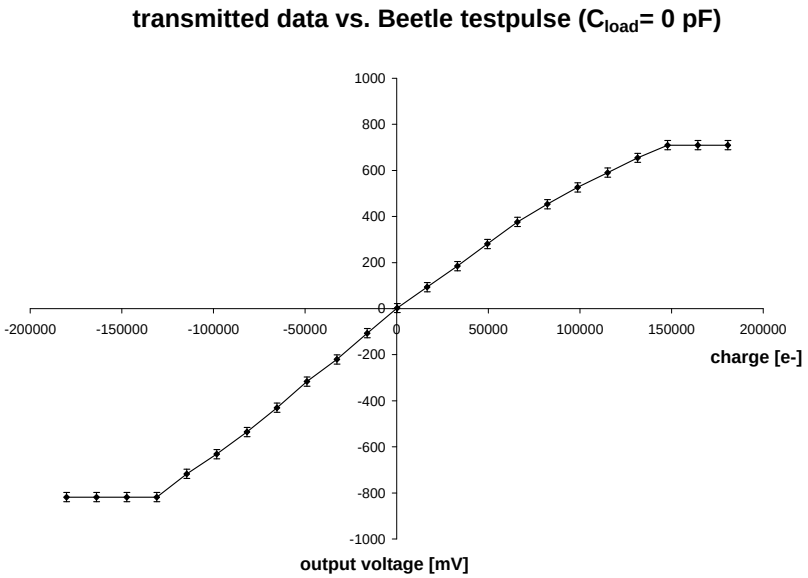

Figure 10.8: Response of the complete optical transmission system for different input charges. The internal testpulse of the Beetle chip was used with a load capacitance of 0 pF. The output voltage was measured after the digital transmission at the output of the DAC.

with good digital signal quality. In addition, the logic transitions of the data were determined to be about 10 ns before the rising edge of the clock, in accordance with GOL specifications that request a minimum of 5 ns. As a single linear clock bus was used for the GOL clock, the variation of the data-to-clock timing was checked for the GOLs closest and farthest to the QPLL device, which is the clock source for the GOLs. The rising clock edge shifts by about 1.5 ns with respect to the data edge. This result is compatible with the expected propagation delay between the GOLs, which are separated by approximately 21 cm.

To test the ADC clock distribution network, which is realized in a tree topology (see Figure 10.11), the clocks of two ADCs at different locations on the board were compared. The measured timing difference of 1 ns most likely originates in part-to-part variations of the LVDS converters used in the clock distribution, but is considered to be negligible (Figure 10.12).

To verify the simultaneous sampling of the ADCs, 16 synchronous LVDS pulse signals were connected to the inputs of the Digitizer Board instead of the Beetle analogue ports. These pulse signals were generated by four DS90LV047ATM quad line drivers. According to their datasheet, the internal propagation delay of those line drivers may shift the phase by max. 1.2 ns, which sets a lower limit on the precision of the measurement. By changing the phase relation between the TESTPULSE and the ADC/GOL clock, the relative sampling times of the ADCs can now be determined by analyzing the clock edges as recorded by the ADCs. The result of this measurement is shown in Figure 10.13. For absolutely synchronous operation

Table 10.1: default operation mode of GOL.

item	name of GOL pin	connected to	configured state
serial transmission mode	conf_glink	GND	Ethernet 8B/10B mode
serial data output	conf_laser	VDD	laserdriver active
GOL data rate	conf_wmode16	GND	'fast mode': 1.6 Gbit/s
data latching clock edge	conf_negedge	GND	data latched on rising edge
PLL charge-pump current	conf_i_pll	GND	10 μA
laserdiode bias current	conf_i_ld$<1:0>$	$<GND:VDD>$	7.4 mA
Ethernet mode error propagation	tx_er	GND	transmitted word is either IDLE or DATA
G-Link flag bits	flag$<1:0>$	both VDD	(ignored in Ethernet mode)
FF0 symbol transmission	FF	VDD	(ignored in Ethernet mode)
clock input selection	selectDiff	VDD	differential input
single ended clock input	clklhc	GND	logic '0', input not used
testshift debug mode	test_shift	GND	standard operation (only used for prototype)

of all ADC channels, all 16 edges should occur at the same time. The measured spread in time is smaller than 2 ns. It can be partially attributed to the different clock timings, as seen earlier, and will certainly contain additional contributions from the internal timing of the ADCs. No clear separation between the channels 0-7 and 8-15 can be seen, despite a difference in trace length of about 4 cm between these two groups. As the duration of the flat top of the Beetle signal is of the order of 15 ns (see Section 7.1), we assume this spread in timing to be negligible.

The digitized data is encoded into 8B/10B Ethernet mode frames compatible to the IEEE 802.3 standard [26]. A high speed VCSEL diode is connected to the GOL's serial output to convert the serialized data into optical signals. The VCSEL is located as close as possible to the GOL package, the 1.6 Gbps signal line being only about 20 mm long. The line is designed with an impedance of 50 Ω to match the impedance of the GOL driving circuit and to improve the signal quality. As the impedance of the VCSEL is only about 25 Ω, a 22 Ω series resistor is used for broadband signal termination.

The VCSEL is a 5 Gbit/s version, capable of delivering up to 0 dBm (1 mW) into a 50/125 μm fibre. It is manufactured by ULM Photonics [31] and is packed in an metal receptacle, which includes an industry-standard SMA fibre interface. As this receptacle is bolted into the Digitizer Board, it provides a robust mechanical fixture for the connected fiber.

To test the overall performance, an eye diagram recorded with higher statistics confirmed the good eye opening and is shown in Figure 10.14.

Synchronization of the optical link is vital not only at the startup of the transmission system, but also during runtime to correct for single event upset induced losses of the synchronization lock. Although the internal logic of the GOL chip is designed in triple redundant logic, a loss of the synchronization lock can still occur. To synchronize on the incoming data

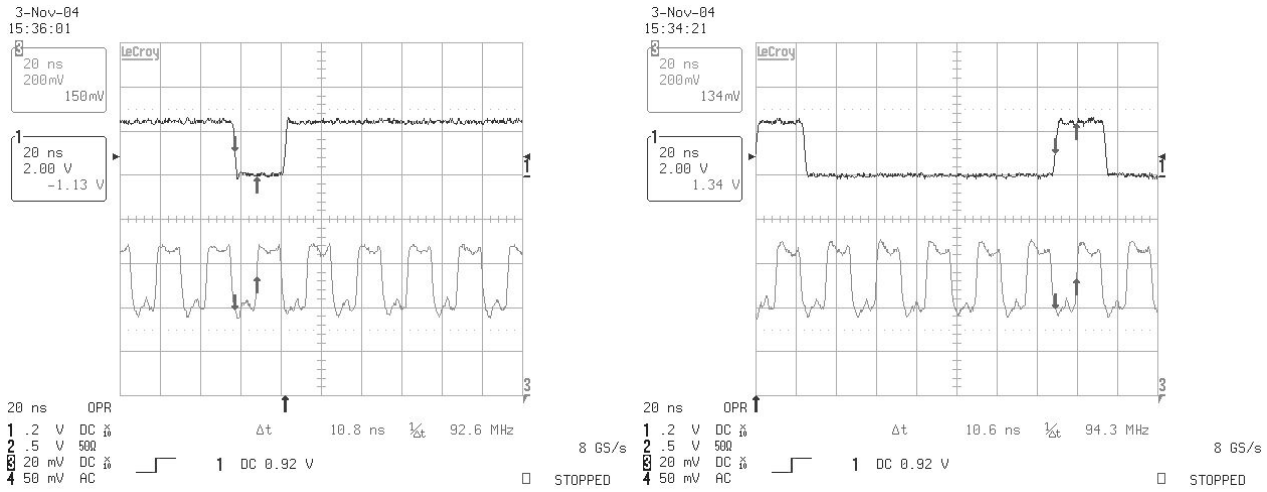

Figure 10.9: Clock-to-data timing relation for an ADC with short (left) and long connections to its GOL, measured directly at the GOL farthest from the QPLL.

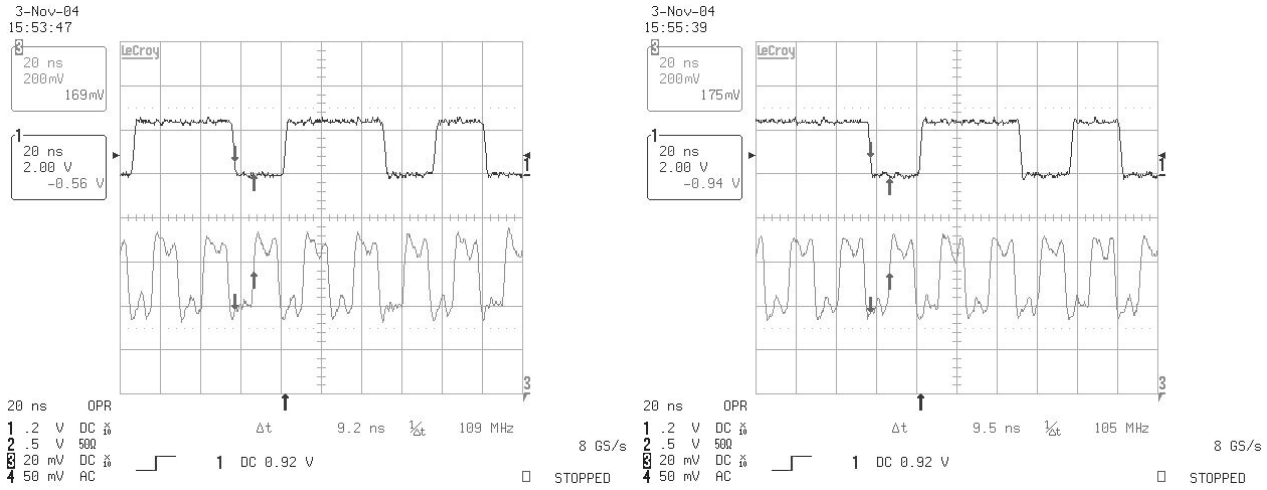

Figure 10.10: Clock-to-data timing relation for an ADC with short (left) and long connections to its GOL, measured directly at the GOL closest to the QPLL.

stream, the TLK2501 needs to receive a specific IDLE frame, which can be generated by the GOL serializer by pulling the TX_EN pin low. If this frame is present at the input of the TLK2501 for at least one transmission cycle, it is able to resynchronize on the data.

An automated solution is implemented to relieve the operator from the need to manually initiate this resynchronization procedure. The Beetle readout chip generates a digital signal, called DataValid, to indicate the presence of analogue readout data. Although the duration of a Beetle readout frame is 36 clock cycles, in compliance with the LHCb L0 electronics specification [9], the DataValid signal is only active for 35 clock cycles to guarantee one clock cycle with no activity, even for consecutive readout. If this digital signal is connected to the TX_EN pin of the GOL, it resynchronizes the serializer during periods without triggers,

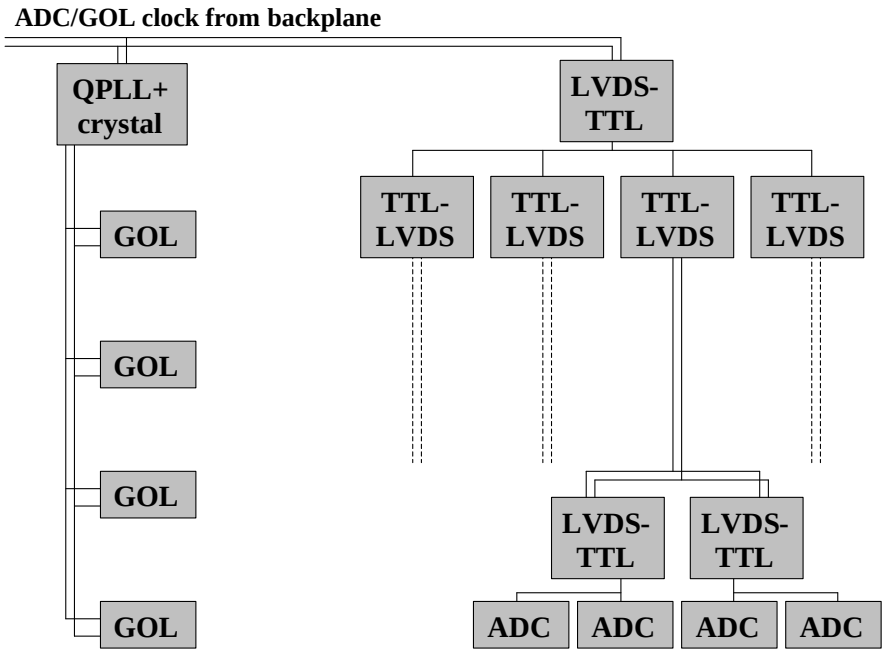

Figure 10.11: Block diagram of the Digitizer Board's clock tree. For simplicity, only one of the four clock trees is drawn completely up to the ADCs.

but at least once every readout frame. Unfortunately, the detector data is delayed by the process of digitization in the ADC and as a result the DataValid signal is not synchronized with the associated readout frame a the input of the GOL. To compensate for this, a shift register which is implemented in an FPGA and clocked by the ADC/GOL clock line is used to delay the DataValid signal. The FPGA is an ex64 antifuse FPGA produced by Actel Inc.[51]. As its internal structure is similar to the A54SX32A antifuse FPGA [52], which has been tested by CERN [53] and NASA [54] for radiation tolerance, we do not expect any problems when this device is exposed to the radiation levels encountered in the LHCb Silicon Tracker environment. To increase its immunity against single event upsets of the shift register, each of its register cells has been implemented with triple redundancy and a majority voting logic. A schematic of a single triple mode redundant register cell is shown in Figure 10.15.

The duration of the DataValid signal is one clock cycles shorter than the standard Beetle readout frame. Therefore, even a correctly shifted connection to the GOL serializer results in the loss of one readout bin. Which readout bin is lost is determined by the delay which is applied to the DataValid signal. As the ADC latency is six clock cycles according to its datasheet and the DataValid is generated by the Beetle chip one clock cycle earlier than the analogue data, a shift of seven clock cycles would lead to the DataValid signal starting in parallel to the digitized readout frame. However, the delayed DataValid would end one clock cycle too early, resulting in the last analogue bin of the Beetle readout not to be transmitted. The DataValid signal is therefore delayed by an additional clock cycle to a total of eight

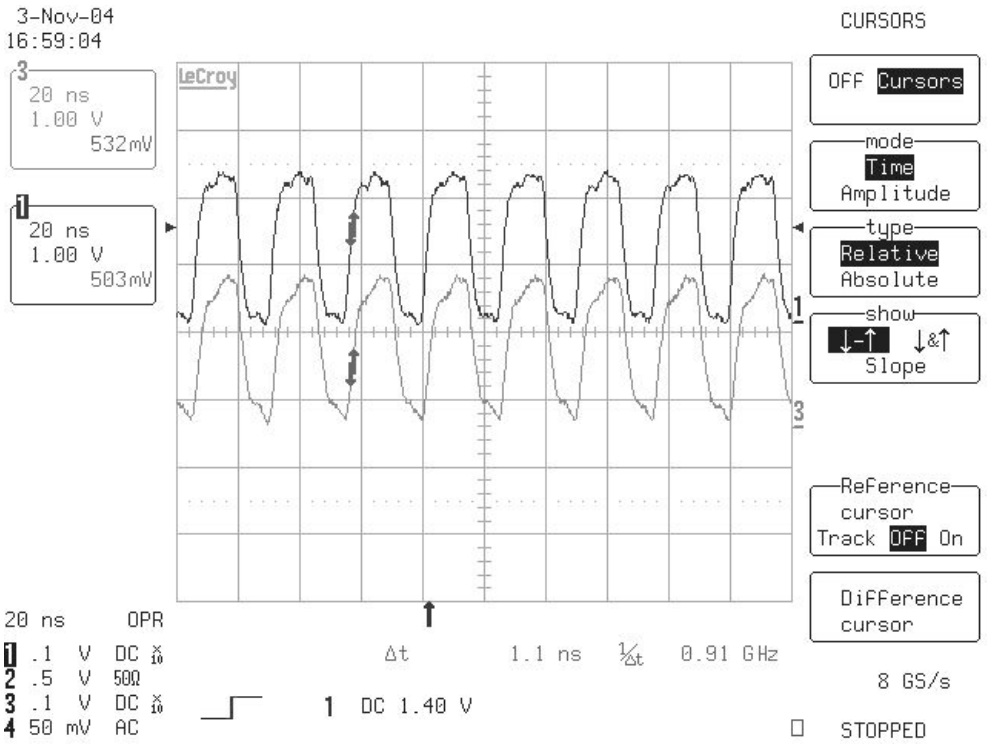

Figure 10.12: Clock-to-clock timing relation for two ADCs located in different corners of the Digitizer board. The time skew is 1.1 ns.

cycles, equal to 200 ns. While all analogue bins are now transmitted, the first bin of the Beetle header on each of the four output ports is not encoded by the GOL serializer. The timing relations are shown in Figure 10.16.

The first header bins on the four Beetle ports are:

- the lead bit, which is always a logic '1',
- the pipeline column number (PCN) parity bit,
- a bit indicating the error detection and correction (EDC) logic being active,
- the parity of the internal Beetle register *CompChTh*.

As the EDC logic is activated by hardwiring a bond pad of the Beetle, the according header bit is supposed to be '1'. The CompChTh parity refers to the comparators which are not used in the Silicon Tracker. The only interesting bit would thus be the PCN parity bit to check for transmission errors of the pipeline column number. This check is however performed anyway in the Level-1 preprocessor board, where the received pipeline column numbers of all Beetle chips are compared to each other and to a local frontend emulator. The information which is lost by delaying the DataValid by eight clock cycles is therefore not considered to be of major importance.

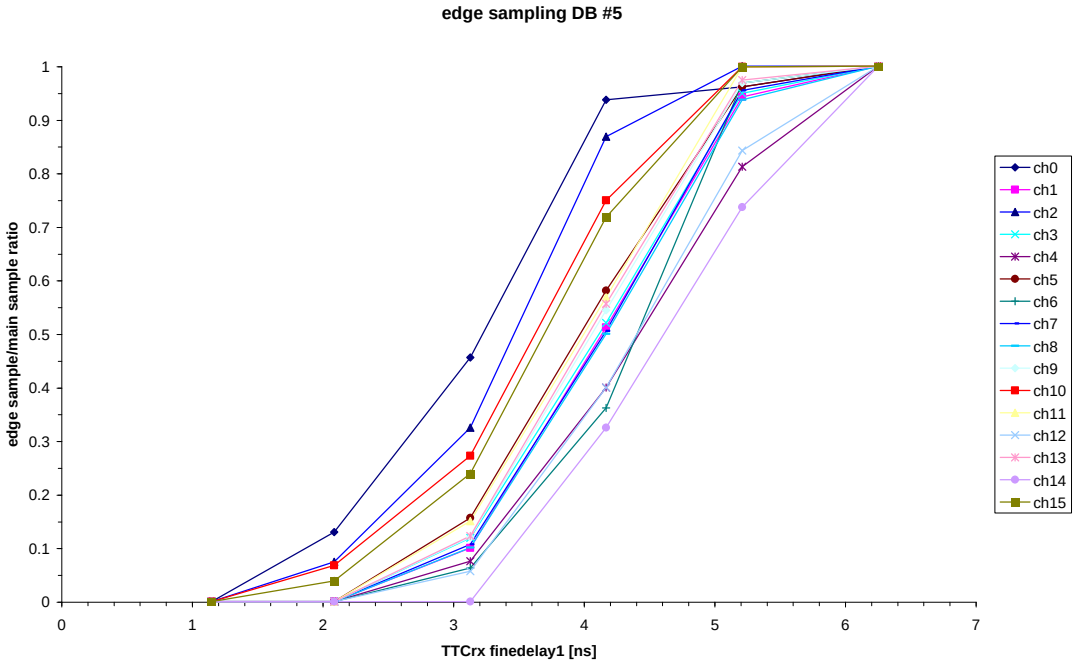

Figure 10.13: Sampled edges of a testpulse, simultaneously applied to all 16 inputs of Digitizer Board no.5. The risetime of 2.4 ns is in agreement with measurements using an oscilloscope.

10.1.2 TTC Signal Distribution

The Timing, Trigger and Control (TTC) network is common to all LHC experiments. It optically distributes the timing information for the LHC beam, which includes the LHC clock with a frequency of 40.079 MHz and the orbit and event counter reset signals. Locally, at the experiments, the L0 trigger and broadcast commands are added to the data stream which is optically distributed to the subdetectors. There, the TTCrx receiver ASIC provides the frontend electronics with the decoded signals.

The LHCb Silicon Tracker frontend hybrid requires neither event nor orbit counter reset signals. The only TTC signals used are the LHC clock, the L0 trigger signal, a testpulse trigger and a L0 reset signal, the last two being encoded by the LHCb readout supervisor under control of the LHCb ECS system. All four signals are supplied to each Digitizer Board from the Service Box backplane. To preserve the signal quality of these time-critical signals, the LVDS standard was used here. These signals are not processed or used on the Digitizer Board. They are routed via impedance controlled differential transmission lines directly to the frontside connector, which connects to the frontend hybrids.

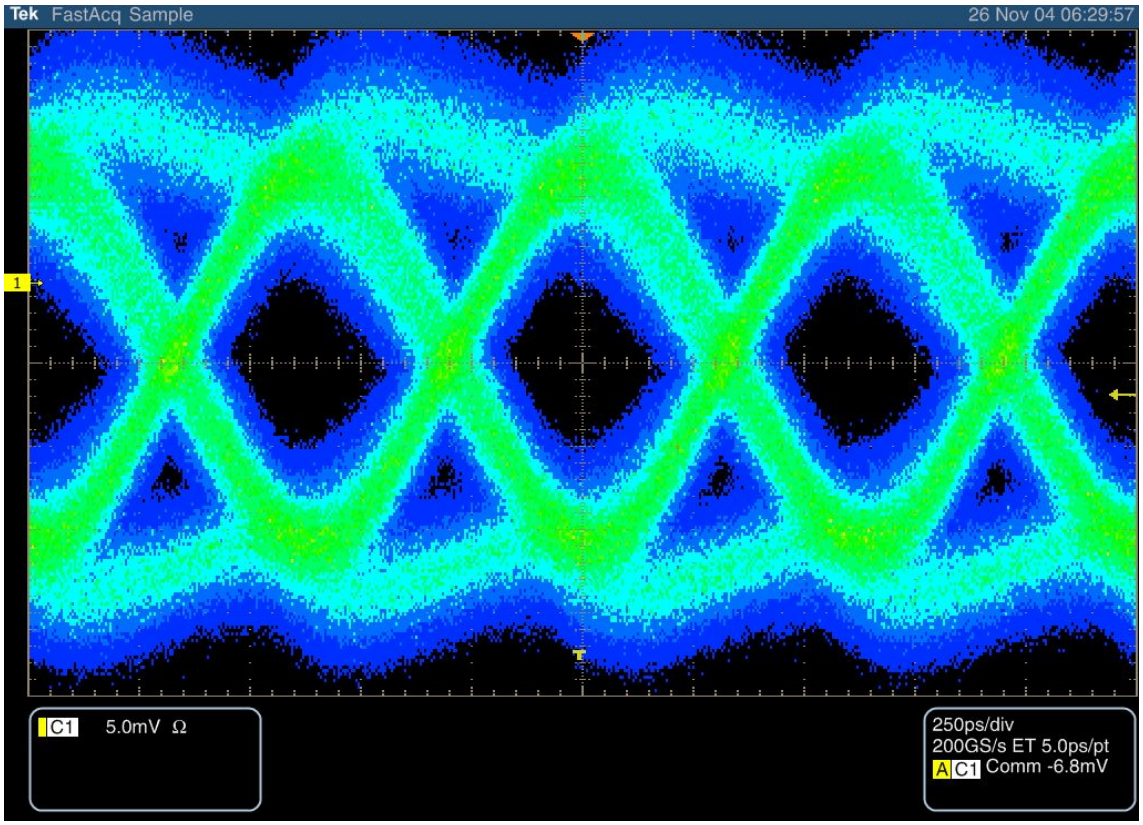

Figure 10.14: Eye diagram of a Digitizer Board channel with a superposition of 10 million waveforms.

10.1.3 Environmental Monitoring

Sensors placed in Service Boxes and Detector Boxes are used to monitor environmental conditions which are relevant for the operational safety, such as temperature and humidity. To digitize the analogue output of these sensors, the DCUF chip from CERN microelectronics [55] is used. Originally developed for the CMS experiment, it is a 6-channel 12 bit ADC designed in the same radiation tolerant technology as the GOL or the Beetle. It includes two current sources (10 μA/20 μA) and an integrated temperature sensor and is accessable via I2C. As one of the analogue inputs is shared with the 20 μA current source output, any use of this source uses up one input channel.

Detector Box A key parameter for the operation of the silicon sensors is their temperature. To reduce radiation induced leakage currents and the associated noise to an acceptable level, the sensors have to be operated at a temperature of around 5 °C [56]. As an individual monitoring of the temperature of each single sensor would require a too complex monitoring system, only the air temperature inside the Detector Box is monitored. This permits to control the proper operation of the cooling systems proper operation. In addition, a humidity sensor will permit to calculate the dewpoint inside the Detector Box. The box will be continuously

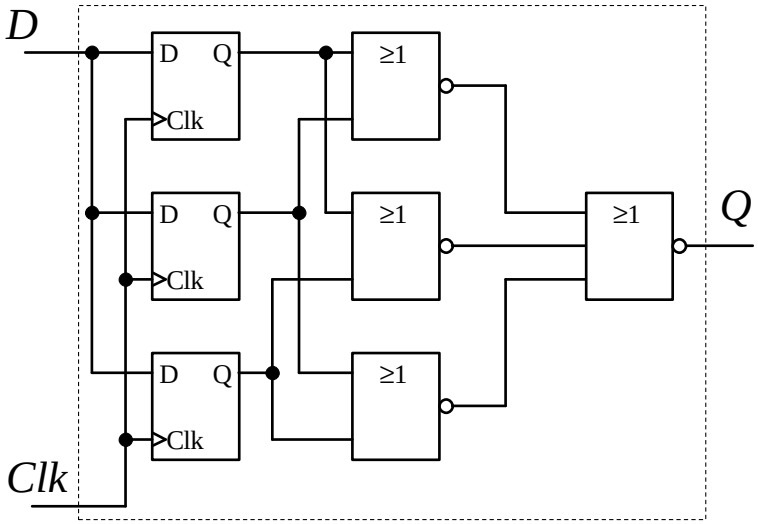

Figure 10.15: Schematics of a triple mode redundant register cell with majority voting.

flushed with dry air to prevent moisture from condensating on cold surfaces. As only a few sensors are needed for this, these parameters will be monitored by a central DCUF, located on the Control Card (see Section 10.2).

Readout Hybrid During Beetle characterization, it was found that some Beetle parameters depend on the working temperature [19]. Although the temperature of the hybrid should be rather constant once thermal equilibrium has been reached, it was decided to include a temperature sensor on every hybrid. As the location of the hybrid is subjected to high levels of ionizing radiation, any integrated digital thermosensors would have had to be radiation qualified. Standard PT1000 sensors are therefore used as they are radiation tolerant due to their simplicity. The PT1000 consists of a platinum resistor with a well defined linear temperature dependence and has a resistivity of 1000 Ω at 0 °C. This high resistivity leads to a low dependence on line resistivity when using a 2-wire measurement. Although a classic 4-wire measurement would completely exclude any effect, a 2-wire design was chosen because of the limited number of available pins on the readout hybrid interface connector.

The PT1000 is located centrally on the readout hybrid (see Figure 10.17) and is connected to the Digitizer Board via two dedicated signal lines of the SCSI cable. It is powered by the 20 μA current source of the DCUF. The voltage drop across the PT1000 is directly proportional to the measured temperature. To amplify this voltage difference, the AD8129 differential amplifier is used. This is the same device that is also used as line receiver for the fast analogue Beetle signals. It is used here, mainly because of its known performance under radiation. As this device has a bandwidth close to 200 MHz, which is much too large for this application, a differential lowpass with a cutoff frequency of approximately 320 Hz is leading its input. The gain of the devices is set to 11, with the operational mode being non-inverting. The inputs are however swapped, so that with the amplifier reference set to 2.5 V, the output

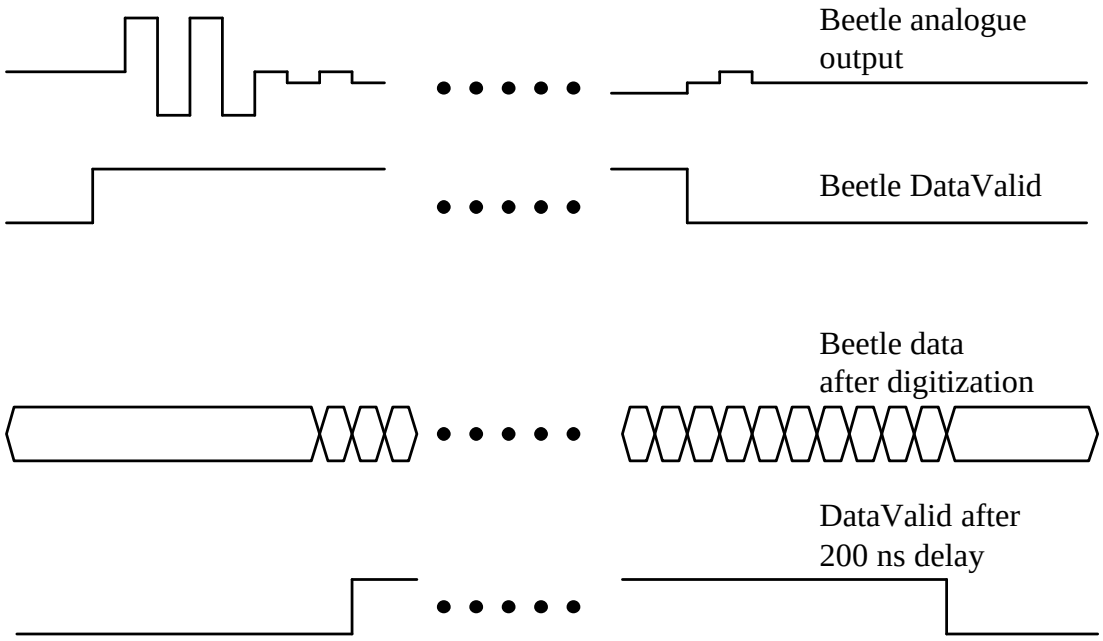

Figure 10.16: Timing relations of the analogue data from the Beetle before and after digitization compared to the DataValid before and after a delay of 200 ns.

voltage is:

$$V_{ampl} = 2.5\ V - 11 \cdot (R_{PT1000} \cdot I_{source})$$

with $I_{source} = 20\ \mu A$, $R_{PT1000} = 1000\ \Omega\ \cdot\ (1 + 0.0039 \cdot \Delta T)$ and ΔT the temperature in °C. The amplified voltage passes a second lowpass filter with a bandwidth of approximately 160 Hz with its output connected to channel 1 of the DCUF on the Digitizer Board. The range mode of the DCUF is set to HIR, which results in possible input voltages of 1.25 V to 2.5 V. Table 10.2 gives some examples for temperatures and the associated digitized values.

Digitizer Board To readout the temperature on the Digitizer Board, the DCUF-internal temperature sensor is used, which can be read out via channel 7. This results in four remaining analogue input channels, which can be used to monitor additional parameters. An important parameter for reliable operation of the GOL serializers is the availability of a low-jitter clock, which is provided by the on-board QPLL. When the QPLL is properly locked onto its input clock signal, the QPLL_READY output is asserted high. This is digital signal is connected

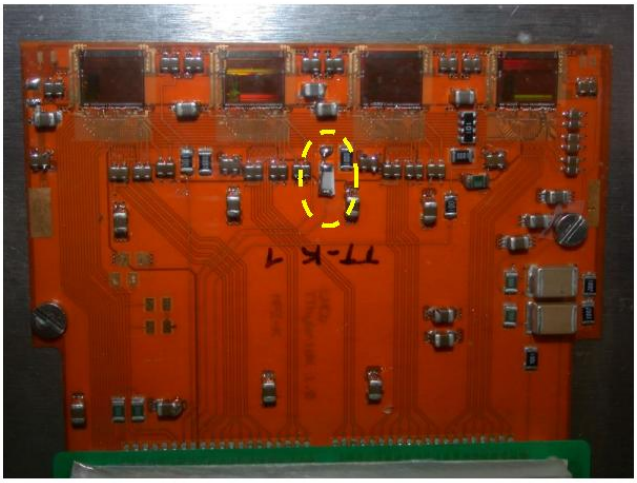

Figure 10.17: Location of the PT1000 on the TT hybrid.

Table 10.2: conversion table T_{PT1000} to ADC bits.

T[°C]	R_{PT1000}	ΔV_{in}	V_{ampl}	ADC bits
-20	922	0.0184	2.297	332
-10	961	0.0192	2.289	346
0	1000	0.0200	2.280	360
10	1039	0.0208	2.271	375
20	1078	0.0216	2.263	389
30	1117	0.0223	2.254	403
40	1156	0.0231	2.246	417
50	1195	0.0239	2.237	431
60	1234	0.0247	2.228	445
70	1274	0.0255	2.220	459
80	1313	0.0263	2.211	473
90	1352	0.0270	2.203	487

to channel 2 of the DCUF to provide a feedback on the proper operation of the QPLL. As the DCUF is a rather slow ADC, any brief losses of lock of the QPLL will not be not detected. Nevertheless, this feedback can be a valuable diagnosis tool in case of sustained loss of serialized data.

The used voltage regulators (see Section 10.3) can signal an overcurrent status via an OCM-signal. If the current limit, which is set with an external resistor, is exceeded, the OCM-signal will be set to a voltage of 0.4 V. Two regulators supply the analogue and digital 2.5 V for each readout hybrid and the corresponding OCM-pins of these regulators are connected to channel 3 and 4 of the DCUF respectively. As the high level of this logic signals is equal to the input voltage of the regulator, resistive dividers are used to protect the ADC from excessive input voltages. The remaining channel 5 is connected with another divider to the

Beetle analogue VDD supply. This voltage is higher than 2.5 V due to the sense topology of the regulator and the line resistivity of the power supply cable to the readout hybrid. Hence, a resistive divider is used here as well. A complete overview of the DCUF channel assignment is given in Table 10.3.

Table 10.3: Channel assignment for the Digitizer Board's DCUF.

channel	connected to	remarks
0	PT1000 sensor on hybrid	20 μA current source
1	temperature sensor	PT1000, amplified by factor 11
2	QPLL locked	
3	OCM pin Beetle VDD regulator	voltage divider 1:5.7
4	OCM pin Beetle VDDD regulator	voltage divider 1:5.7
5	Beetle VDD voltage	voltage divider 3.3:4.3
6	DCUF bandgap voltage	internally connected
7	DCUF temperature	internally connected

10.1.4 Slow Control Signal Distribution

In the Silicon Tracker, the I2C protocol is used to control and monitor the frontend systems. As the line capacitance of each I2C bus, and therefore the line length, is limited, its use is restricted to the communication between each frontend hybrid and its associated service box. The subdetector-wide communication proceeds via the SPECS system, as described in Section 9.2.

For safety reasons and to limit the number of devices on a single I2C bus, the Beetle I2C bus was completely separated from all other I2C devices. This also allows for instant programming of all Beetles on a given I2C bus by an I2C general call. The non-Beetle I2C bus contains the GOL and the DCUF chips. Communication on this bus will be dominated by the readback of the DCUF data, as the GOL should need little or no intervention for startup.

It was decided to group at maximum 4 readout hybrids into a single I2C section to limit the number of devices per I2C bus. Each section contains a Beetle bus and a GOL/DCUF bus. For a unique device identification, the I2C identifier of all chips will be determined by hardwiring address pins. As some of the bits of the devices are used internally for register access (see Figure 10.18), only a subset of the 112 possible addresses of the I2C protocol may be used.

For the Beetle chip, all seven I2C address bits can be used. Its programming scheme only occupies a single address on the I2C bus despite having several internal registers to write. The GOL chip occupies two addresses on the I2C bus, as the first address is associated to the register pointer and the second to the selected register content. The DCUF chip needs the three least significant bits to distinguish between its eight internal registers. For a user defined addressing scheme, this leaves only the address bits A6 to A3.

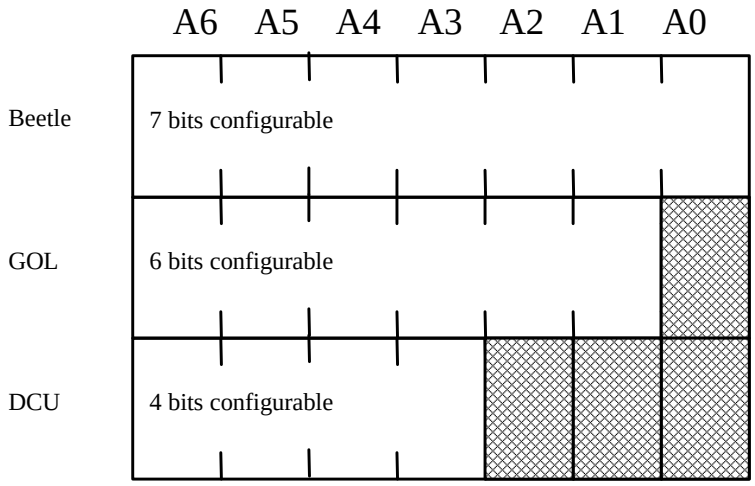

Figure 10.18: Possible addresses for used I2C devices. Shaded address bits are used internally by the according device.

The I2C address ranges '1' to '7' and '120' to '127' are reserved by the I2C standard (see [17]) and must not be used. The address '0' is reserved for the 'general call', which addresses all I2C devices on a bus at once. As a result, only the adress range '8' to '119' is free for use.

As each readout hybrid is associated with a Digitizer Board, a **Board-ID** is defined, ranging from 0 to 3 and set by the I2C address bits A6 and A5. All devices (Beetle, GOL, DCUF) linked to a specific board will be programmed with the same Board-ID. This is done with the common lines I2C_ADR5 and I2C_ADR6, which are connected to all I2C devices. The logic state of these lines is determined for each Digitizer Board and its associated readout hybrid by the backplane slot, in which the Digitizer Board has been placed. With this scheme, all Digitizer Boards can be produced identically without the need for manual addressing before installation and double address associations are avoided.

For the GOL/DCUF I2C bus, address Bit A4 determines the device type, where '1' is associated with a GOL chip and '0' with a DCUF. While the GOL address range is now compliant with I2C standard, the DCUF address can still be in the range of 0-7 (bits A6-A3 all '0'), which is not allowed according to I2C specifications. Address bit A3 is hardwired to '1' for all DCUF devices to avoid this conflict. The use of the A3 bit of the GOL is not limited by the I2C protocol and it is permanently connected to '0'. While for the DCUF, all user definable address bits are fixed by this definition, the GOL bits A2 and A1 can still be selected. They are used for the **Chip-ID**, ranging from 0 to 3, which corresponds to the consecutive numbering of the Beetle chips on a given hybrid. This is compatible for both versions of the Digitizer Board, with three GOLs for the IT version and four GOLs for the TT version. In addition, associating bits A2 and A1 on the readout hybrid to the four Beetle readout chips creates identical addresses for each Beetle/GOL pair. No address conflict occurs since the

I2C buses are held separate. As the bit A0 is used for programming internal GOL registers, the matching of addressed can not be extended to the full I2C address. The remaining bit A0 of every Beetle is connected to '0' as no further addresses are needed for the Beetle I2C bus.

The final address assignment is shown in Figures 10.19, 10.20 and 10.21.

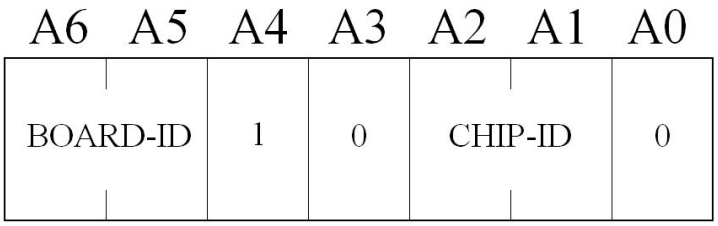

Figure 10.19: Beetle I2C address definition.

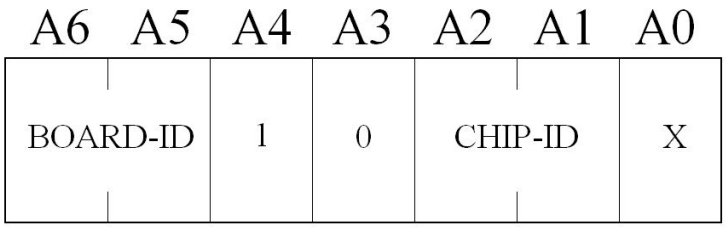

Figure 10.20: GOL I2C address definition. 'X' bits are used internally.

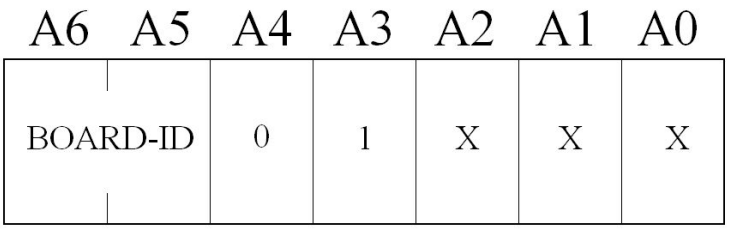

Figure 10.21: DCUF I2C address definition. 'X' bits are used internally.

10.2 Control Card Design

A single Control Card serves as the central point for TTC and ECS signal distribution in each Service Box. The design for the Control Card is still under development, but its basic requirements have been defined. A block diagram is shown in Figure 10.22.

The Control Card has to provide:

- TTC signals: LHCclock, L0trigger, L0reset, trigger for testpulses
- ECS signals: I2C command buses, parallel I/O lines
- analogue inputs for detector box environment monitoring (humidity, temperature)

To generate these signals, two plug-in units are used: the TTCrq mezzanine, designed by CERN microelectronics group, and the SPECS slave mezzanine, designed by the LHCb calorimeter group at LAL Orsay.

The TTCrq mezzanine is a plug-in board consisting of a photodiode for connection to the optical TTC network, a TTCrx chip (see Section 9.1) and a QPLL low-jitter PLL chip to stabilize the LHC clock for use with the GOL chip. The TTCrq still has to be modified as two components (voltage regulator and LVDS-TTL converter) are not radiation qualified. These components however do not affect the functionality used by the Control Card and they can be simply removed from the mezzanine to prevent any problems.

The SPECS slave mezzanine is based on an ACTEL 54AX250 antifuse FPGA and has been radiation qualified up to 40 krad of total ionizing dose [60]. It provides eight I2C or JTAG buses and 32 general purpose TTL I/O lines, which can all be controlled separately.

The TTC signals are simply fanned out from a single TTCrq, so that there is no limit on the number of Digitizer Boards. The number of needed required SPECS slave mezzanines depends on the number of needed I2C buses and I/O lines per Service Box.

Four Digitizer Boards are foreseen to share two I2C buses, one for the associated Beetle frontend chips and one for the GOL/DCUF devices (see Section 10.1.4). For 16 Digitizer Boards, as planned for the Service Box, eight I2C buses would therefore be required, which is compatible with one SPECS slave mezzanine. The eight bus lines are not directly provided by the SPECS slave, but have to be created by using eight bus select lines from the SPECS slave to control external bus switches. The realization of these bus switches has yet to be determined, with two options being available. One option simply uses a combination of radiation qualified LVDS transceivers to switch among the buses with the enable pins provided by the transceivers themselves. The other option is the use of a small radiation-tolerant antifuse FPGA, similar to the one used for gigabit link synchronization on the Digitizer Board.

A key requirement for the ECS system is the possibility to power down individual readout hybrids. This implies the shutdown of two low-voltage regulators (analogue/digital). These voltage regulators are implemented on the backplane and each pair can be controlled by a single TTL line. For a complete Service Box, this requires 16 TTL lines.

There also exists the possibility to power down Digitizer Boards. As four Digitizer Boards share not only an I2C bus, but also a 5 V regulator for the line receivers, each group of four Boards can be power cycled individually. This requires another four TTL lines.

As the overcurrent monitoring pins (OCM) of the low-voltage power regulators for the Beetle chips are already monitored by the DCUF on the Digitizer Board, the only remaining OCM lines are those of the regulators supplying the Digitizer Boards itself. Each group of four boards is supplied by two 2.5V regulators, one 5 V and one 3.3 V regulator. In total, this results in 16 OCM-pins that need to be monitored via 16 TTL lines.

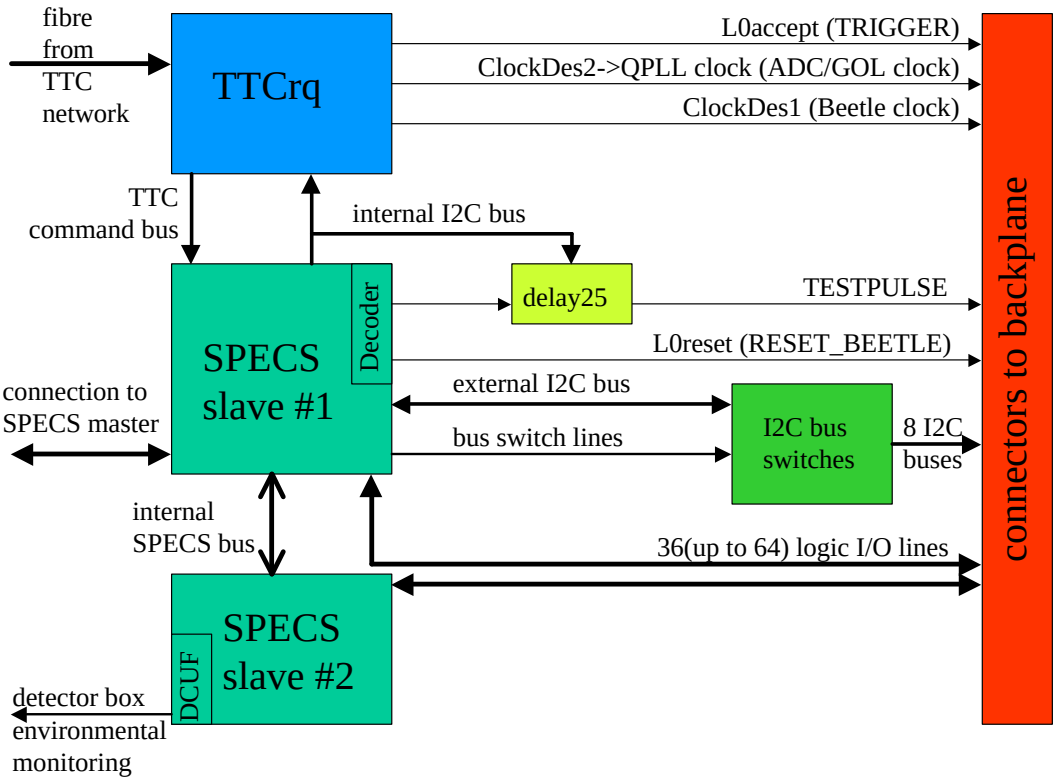

Figure 10.22: Blockdiagram of the Control Card.

To sum up, a Control Card for 16 Digitizer Boards needs to control eight I2C buses and 36 TTL lines. This requires a minimum of two SPECS slave mezzanines. Each Control Card thus carries one TTCrq and two SPECS slaves. In addition, a delay25 device is implemented that permits to shift the phase of the TESTPULSE signal with respect to the Beetle clock and thus perform pulseshape scans of the readout amplifier. This device has been developed by the CERN microelectronics group for CMS [57] and is radiation tolerant, as it is based on the same process as the Beetle and the GOL chip.

10.3 Backplane Design

The Service Box backplane is used to distribute the slow control and TTC signals between the Control Card and the Digitizer Boards. Located on the backplane are also the radiation

hard linear voltage regulators, which provide the Digitizer Boards and frontend hybrids with regulated supply voltages. The backplane is mounted onto a cooling block that serves to remove the heat generated by the power regulators, which have a typical power efficiency of about 50%.

TTC Signals The TTC signal distribution consists of the clock trees for the ADC/GOL devices and the Beetles, the L0accept, the L0reset and the testpulse trigger signal. As the timing of all of these signals is critical, LVDS is used throughout the backplane. With the Control Card being the only signal source and the up to 16 Digitizer Boards being the signal receivers, a strict tree structure was designed, with exactly one receiver per differential line. All differential lines are designed to have an impedance close to 100 Ω to ensure proper signal transmission and termination. To fan out the single signal sources to multiple receivers, the DS90LV047 quad differential LVDS driver was used in conjunction with the DS90LV048 quad LVDS receiver. Both devices have been tested by ATLAS up to a total ionizing dose of 70 krad without any failures [53], which qualifies these devices for use in the Service Box environment. A 1:4 fan out for the TTC signals is shown in Figure 10.23. A group of four LVDS signals is distributed by converting the signals to TTL in a DS90LV048 receiver, which is connected to four DS90LV047 line drivers that are located nearby. These convert the signals back to LVDS standard. Four time-critical TTC signals have to be distributed to each Beetle readout hybrid.The four signals are converted in a single device, as channel-to-channel skew is minimized. A similar clock tree distributes the 40 MHz ADC/GOL clock, whose phase is independently adjusted by the TTCrx (see Section 10.2).

By concatenating two of these fan out designs, each backplane is able to provide up to 16 Digitizer Boards with fast TTC Signals. By placing the Control Card in the center slot of the backplane, trace length differences can be minimized. This is of particular importance, since equal phase relations on all 16 Digitizer Boards have to be ensured by the layout of the backplane. No option is foreseen for the user to fine-tune timing relations between different Digitizer Boards. As the detectors that are read out through a single Service Box are geometrically located close to each other, it is assumed that the time difference between the particles crossing the detectors can be neglected. The sampling point for the whole group of detectors can be adjusted using the clock delay lines in the TTCrx, as described in Section 9.1.

Slow Control In addition to the TTC signals, the Control Card also provides slow control signals to the Digitizer Boards. They contain the I2C buses to the readout hybrids, the I2C buses to the GOLs and the DCUF on each Digitizer Board, and two reset lines: one for the GOL and one for the QPLL. While both of these devices could in principle be tied locally via an RC-network to the supply power to provide a power-up reset, it was decided to have both reset lines controllable via the ECS system. As the exact timing of the GOL reset might be relevant at some point during operation, it is transmitted by LVDS signals to the Digitizer Boards. For the QPLL operation, the exact timing of the reset signal has no meaning and it was therefore decided to connect all QPLLs to a common reset line, which can be triggered by the Control Card.

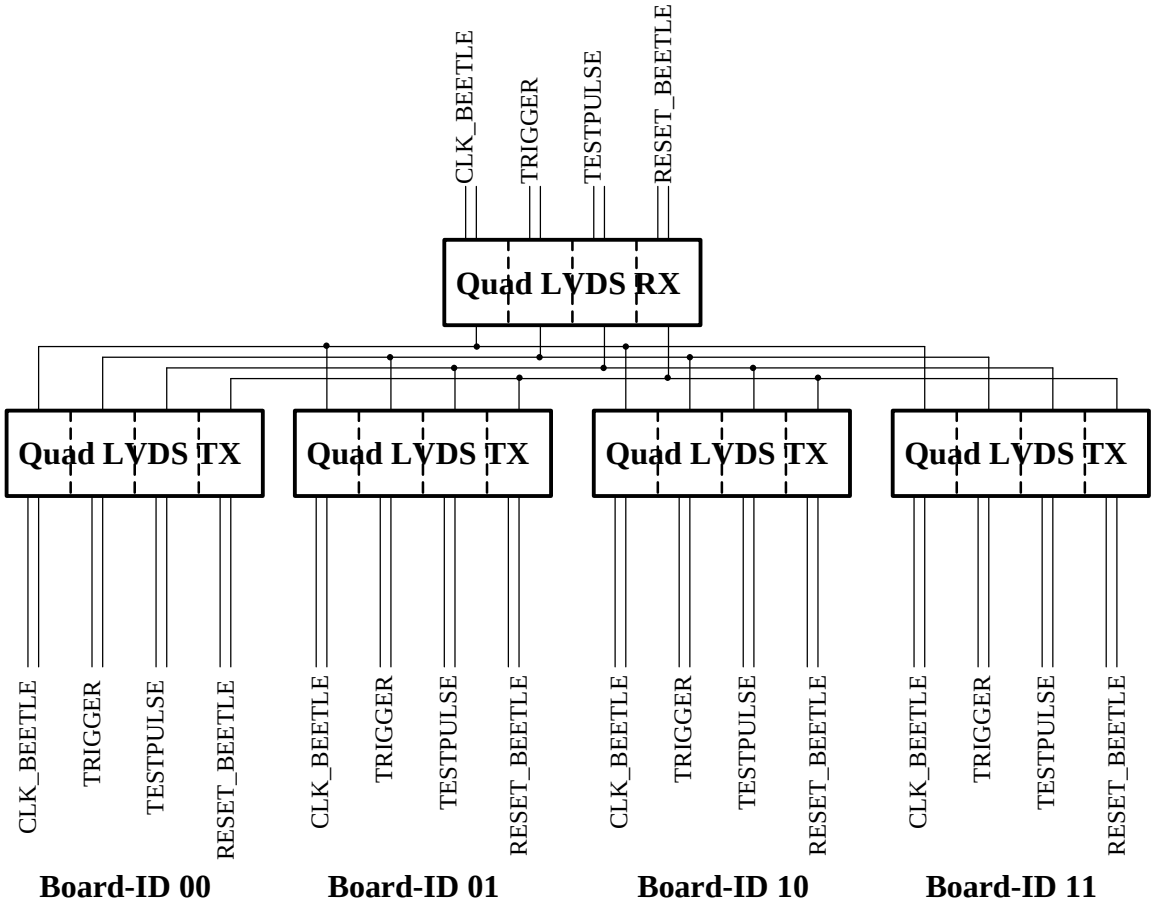

Figure 10.23: 1:4 fan out of the TTC signals, as implemented on the backplane.

The I2C addressing scheme (see Section 10.1.4) contains two bits, labeled Board-ID, which assign part of the I2C addresses to the bus devices. These two bits are set by plugging a Digitizer Board into a slot of the backplane, as the corresponding pins of the backplane connector are hardwired to ensure a unique address for each I2C bus. The Board-ID partitioning for the backplane prototype is shown in Figure 10.24.

Voltage Regulators The L4913 positive voltage regulator has been developed by the CERN microelectronics group and is designed to withstand high radiation levels [58]. The device supports the output voltage to be adjustable between 1.23 and 9 V. The L4913 supports the use of sense lines for voltage regulation directly at the load. While the regulator is rated for a maximum current of 3.2 A, a lower current limit can be set with an external resistor. However, it has to be noted that the regulation quality decreases when the current drawn exceeds 66% of the maximum current set. In case the limit itself is reached, the regulator will signal this by pulling its OCM pins low. An INHIBIT pin allows to shut down the voltage regulator with a logic signal. More information can be found in the L4913 datasheet [58].

Intensive testing during sample characterization showed that the voltage regulator tends

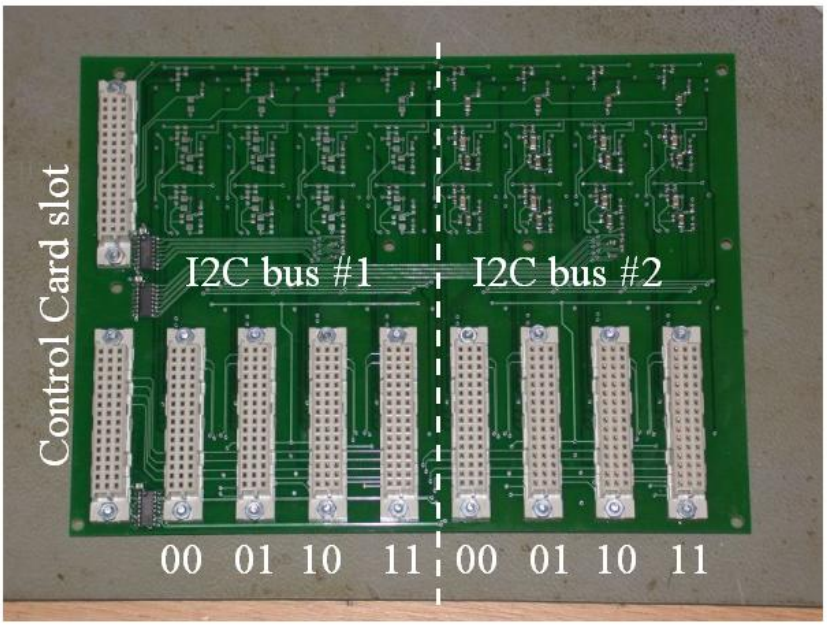

Figure 10.24: I2C Board-ID on the backplane prototype (50 % of full backplane).

to oscillate under certain operating conditions. This oscillation had a frequency around 1 kHz and a voltage amplitude of about 0.5 V and more. A 1 μF ceramic capacitor between the regulator output pin and the positive sense line was found to suppress these oscillations for all tested cable types and lengths. The typical schematic diagram showing the use of a 2.5 V regulator on the backplane is shown in Figure 10.25. A more detailed description can be found in [59].

In the Silicon Tracker on-detector electronics, voltages of 2.5 V (all deep-submicron devices), 3.3 V (backplane clock distribution network) and 5 V (Digitizer Board clock distribution, line receivers and TTCrx photodiode) are needed. The partitioning of the loads has not only to follow a logic grouping, but has to take in account the maximum current that can be regulated by a single voltage regulator. Each Beetle hybrid has its own set of regulators with their associated sense lines to supply 2.5 V to the Beetle readout chips. This permits to switch off individual hybrids. To minimize crosstalk between the analogue and the digital part of the Beetle readout chip, each hybrid is connected to separate analogue and digital regulators. For an efficient use of the regulators, it was decided to supply more than one Digitizer Board from a single regulator. According to the current requirements, as listed in Table 10.4, it is possible to supply two Digitizer Boards from a single 2.5 V regulator and up to five Digitizer Boards from a 5 V regulator. As the partitioning I2C buses results in groups of four Digitizer Boards each, it was decided to map the same partitioning to the power supply, sourceing four Digitizer Boards from one voltage regulator set, containing two 2.5 V regulators and one 5 V regulator. As each of Digitizer Board groups is supplied with

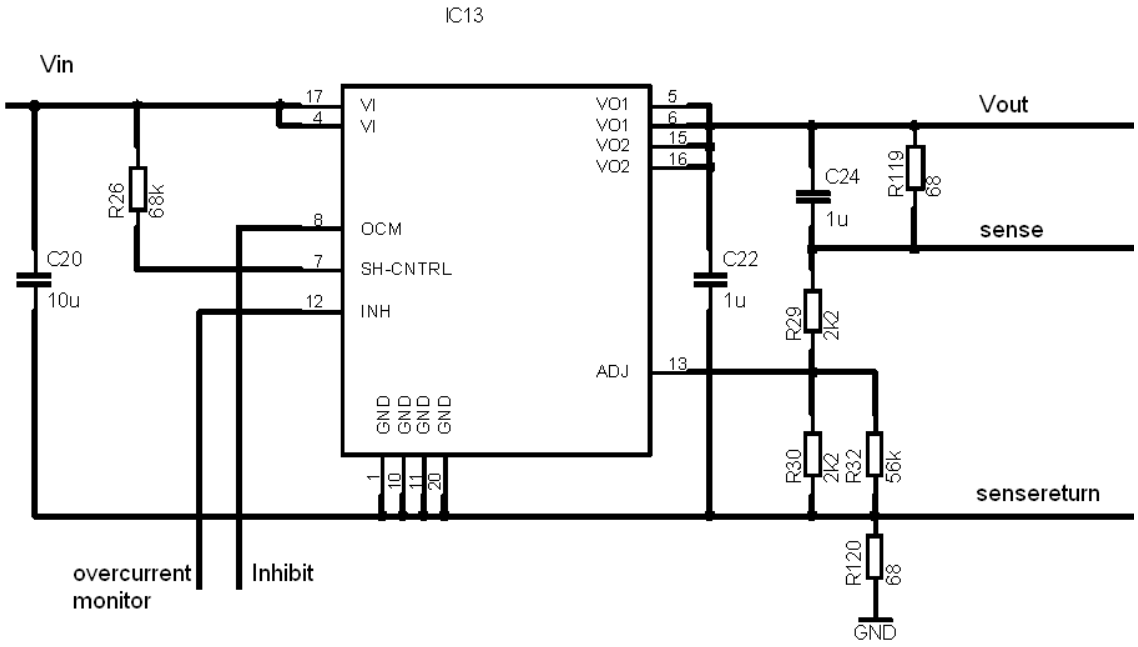

Figure 10.25: Schematic diagram for a 2.5 V regulator.

its own branch of the backplane clock distribution network, a 3.3 V regulator was included in the voltage regulator set as well. As a result, a regulator set supplying a group of four Digitizer Boards/readout hybrids contains:

- four analogue and four digital 2.5 V regulators (four Beetle hybrids), max. 0.8 A/0.2 A each
- two 2.5 V regulators (deep submicron devices of four Digitizer Boards), 2 A each
- one 3.3 V regulator (backplane clock branch), 185 mA
- one 5 V regulator (line receivers and clock tree of four Digitizer Boards), 1.6 A

The L4913 regulator is packaged in a special PowerSO-20 case to minimize the thermal resistivity from the die to the heatsink. As this metal slug is connected electrically to the local ground of the regulator, which may be different for the regulators using the sense line topology, this slug must be kept electrically isolated from the heatsink. All regulators are located on the back side of the backplane (see Figure 10.26), as the Digitizer Boards will be inserted from the front side. It is therefore possible to cool all regulators with a common flat water-cooled heatsink.

To minimize the power losses due to excessive input voltage, the inputs of all regulators are grouped according to their regulated output. While connecting all 2.5 V regulators together

Table 10.4: required voltages and currents for on-detector electronics.

item	location	number of units per location	supply voltage	total supply current
Beetle	readout hybrid	4(3)	2.5 V analogue 2.5 V digital	800(600) mA 200(150) mA
TSA0801 ADC	Digitizer Board	16(12)	2.5 V	256(192) mA
GOL	Digitizer Board	4(3)	2.5 V	640(480) mA
QPLL	Digitizer Board	1	2.5 V	40 mA
DCUF + ex64	Digitizer Board	1+1	2.5 V	12 mA + 8 mA
		2.5 V total	per Digitizer Board	956(732) mA
AD8129 line receiver	Digitizer Board	17(13)	5 V	187(143) mA
DS92LV010 clock distribution	Digitizer Board	15	5 V	195 mA
		5 V total	per Digitizer Board	382(338) mA
DS90LV047A quad LVDS driver	backplane	30	3.3 V	600 mA
DS90LV048A quad LVDS receiver	backplane	16	3.3 V	144 mA
		3.3 V total	per backplane	744 mA

leads to an almost identical voltage drop across all regulators, it was decided to combine the inputs of the 3.3 V and 5 V regulators together. Although this leads to a rather high voltage drop for the 3.3 V regulators, the dissipated power is rather low due to the low current needed by the 3.3 V loads. This design reduces the number of different input voltages for the Service Box to two: about 4.5 V are needed for the 2.5 V regulators and 6 V are needed for the 3.3 V and 5 V regulators. The higher voltage drop for the 2.5 V regulators is needed to compensate for the higher line resistance for supplying the readout hybrids.

Figure 10.24 and 10.26 show a prototype backplane for eight Digitizer Boards. It is designed in a 4-layer technology and has controlled impedance traces for the LVDS signals. During testing, the supply lines were determined to have a too low cross section, leading to too high voltage drops. As a temporary fix, the supply traces were bridged manually to reduce the voltage drop. To correct this for the final version of the backplane with 16 slots, the design will be upgraded to 6 layers with enough board area for large supply trace cross sections.

10.4 Service Box Mechanical Design

The mechanical design of the Service Box was primarily driven by the limited space available at the tracking stations T1-T3 of the Inner Tracker. The overall height of the box had to be limited to 160 mm. This influenced the basic design of the Digitizer Board by limiting its height to 140 mm. The second dimension of the box is determined by the length of the

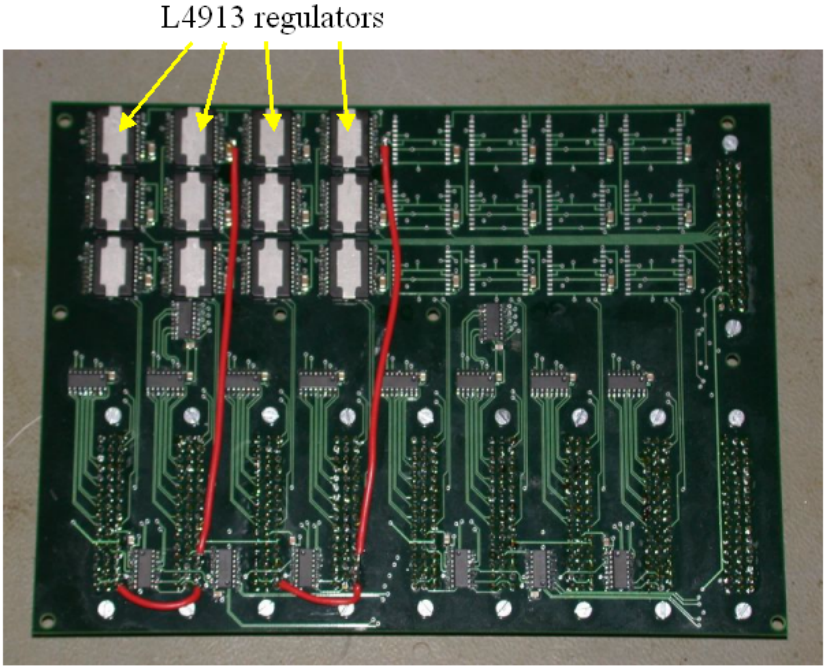

Figure 10.26: View of the backplane regulators (backplane only partially equipped).

Digitizer Boards in direction of insertion, which is 328 mm. Another 20 mm have to be added for the backplane and 15 mm for the copper heatsink, resulting in a total depth of 365 mm. The third dimension is based on the slot interval, which was fixed to 20 mm to provide sufficient space between the VCSEL diodes on the Digitizer Board. As the Service Box holds 16 Digitizer Boards plus 1 Control Card, the minimum width is 320 mm. Another 40 mm are added on each side for a patch panel with MTP connectors, where the breakout fibres joining the single fibres from the VCSEL diodes are connected to the 12-channel ribbon fibre leading to the counting house. This sums up to a total width of the Service Box of 400 mm.

The pipes for supplying the heatsink with cooling water as well as the low voltage power supply are connected to the back side of the box. The SCSI cables connecting to the readout hybrids are plugged into the input connectors of the Digitizer Boards on the front side. The single fibres which are connected to the VCSEL diodes are routed inside the Service Box to the patch panels on each side of the Service Box, where they are joined to 12-channel fibre ribbon cables. The weight of a fully assembled Service Box is approximately 9 kg, which simplifies manual handling and assembly into the LHCb structure.

Figure 10.28 shows a photograph of the Service Box prototype. It features only eight Digitizer Boards, as it is based on the prototype of the backplane described earlier. The empty slot on the right is reserved for the Control Card. The patch panel on the left can hold up to three MTP interfaces for the optical fibre ribbon cables.

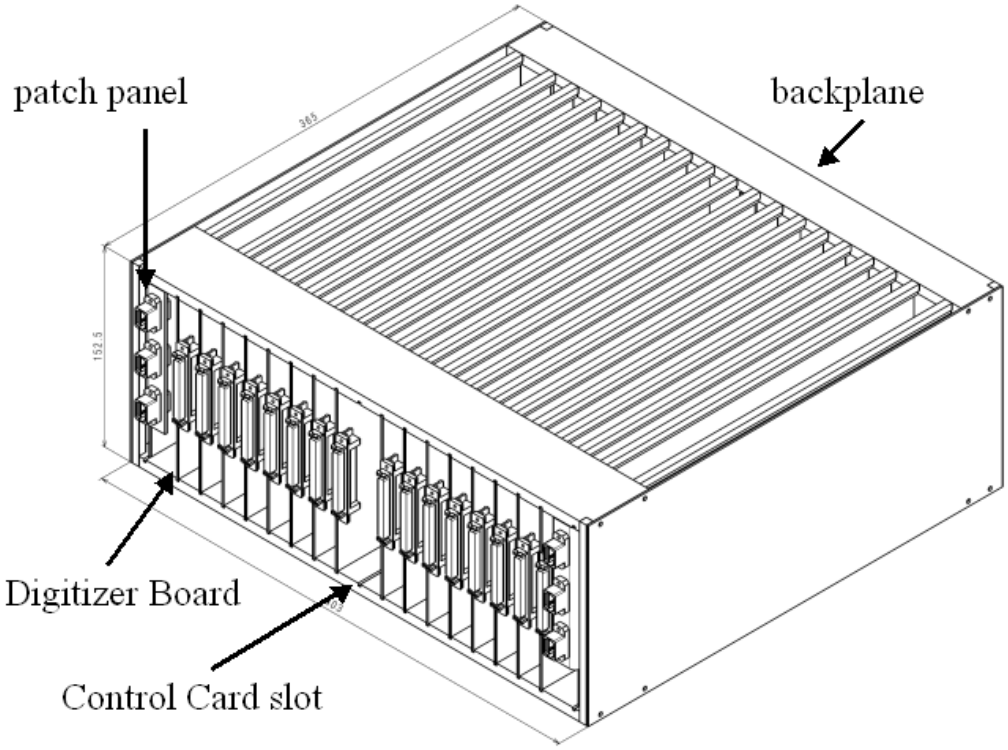

Figure 10.27: Mechanical drawing of a 16-slot Service Box.

10.5 Power Dissipation

The power dissipated by the Service Box components has to be evaluated to estimate cooling requirements and operational temperature. This is not only important to ensure that none of the components needs extra cooling but also as input for the LHCb infrastructure group, as the overall heat introduced by the complete detector into the ambient air has to be extracted by the air conditioning system to prevent overheating of the experimental area.

Table 10.5: voltages and currents for a TT Service Box with 16 Digitizer Boards + Hybrids.

regulated voltage	Service Box total current	dropout voltage of regulator	regulator dissipated power	total power
2.5 V	32 A	2 V	64 W	144 W
3.3 V	1 A	1 V	1 W	4.3 W
5 V	6.4 A	1 V	6.4 W	38.4 W

The power dissipation of the individual components can be extracted from Table 10.4. Grouped according to voltages, the currents for a total Service Box loaded with 16 Digitizer Boards are listed in Table 10.5. As approximately 70 W are dissipated by the regulators, which

Figure 10.28: Photograph of the Service Box prototype.

are located close to each other on the backplane, a water-cooled heatsink is needed there. The power dissipated by each Digitizer Board is below 5 W, with the GOL power dissipation of 400 mW being the hottest spot on the board. As a result, the Digitizer Boards do not need cooling in addition to convective cooling by the ambient air. Air convection is made possible because of the open design of the Service Box (see Figure 10.27). Further thermal testing with the fully populated Service Box prototype is planned to verify the operational temperatures.

10.6 Detector Partitioning

This sections presents a proposal how to distribute the readout of Trigger Tracker and the Inner Tracker to the numerous Service Boxes. As the distance between the readout hybrids and the Service Boxes is limited to a cable length of 5 m, the location of the Service Boxes relative to their associated hybrids has to be taken into account in the partitioning.

10.6.1 Trigger Tracker

For the Trigger Tracker, the four layers of the complete subdetector are very close to each other, with the TTa and TTb section separated by only 30 cm along the beampipe. With

particles, which have to be recorded, moving with a velocity close to the speed of light, the resulting timing difference when passing the two sections is in the order of 1 ns. As a consequence, all detectors can be read out using the same readout clock and a single Service Box can process data from all four layers. Connecting four readout areas covering the same location in x-y should be avoided to prevent a total loss of tracking information in case a Service Box should experience a failure. For installation and maintenance, the TT station is split into a left and a right half, which can be pulled away from the beampipe. Any Service Box should only process data from readout hybrids of one detector side to avoid excessive cabling. As the Trigger Tracker has a total of 280 readout hybrids, each side has to be equipped with Service Boxes capable of handling 140 hybrids. Upper and lower boxes should not be mixed into the same Service Box to avoid long cables. Therefore, the readout is separated into quadrants. When summing up all readout hybrids per quadrant, each quadrant includes exactly 70 hybrids, so that five Service Boxes with 16 slots are required to read out each quadrant. The total number of needed Service Boxes for the TT is therefore 20.

The exact location of the boxes was chosen according to two major design constraints:

- cables to the readout hybrids should be no longer than 5 m,
- the total ionizing dose must be less than 15 krad for 10 years of LHC-operation.

Additional constraints have to be taken into consideration, such as availability of space, accessability and the need to provide mechanical support structures. The final location of the TT Service Boxes still needs to be defined. One option that is being considered is to locate the Service Boxes at the outer beams of the Trigger Tracker support structure, as shown in Figure 10.29. Based on background simulation data from May 2003 [36], the maximum total ionizing dose at this location was determined to be 13 krad for 10 years of operation, including a safety factor of two to account for simulation uncertainty.

10.6.2 Inner Tracker

As the three Inner Tracker stations are located on different support structures and each of these structures is divided in half to allow opening of the station, similar to the Trigger Tracker, it was decided to associate the Service Boxes to the moving support structures, each of which holds two detector boxes from a single tracking station.

The two detector boxes hold 28 sensor ladders each , which requires four Service Boxes. To simplify the mapping of Service Boxes to detector boxes, each Service Box is going to read out 14 hybrids. This leaves two free slots in each Service Box, which can be used as spares. In total, the Inner Tracker needs 24 Service Boxes. Figure 10.30 shows the proposed location for the Inner Tracker Service Boxes.

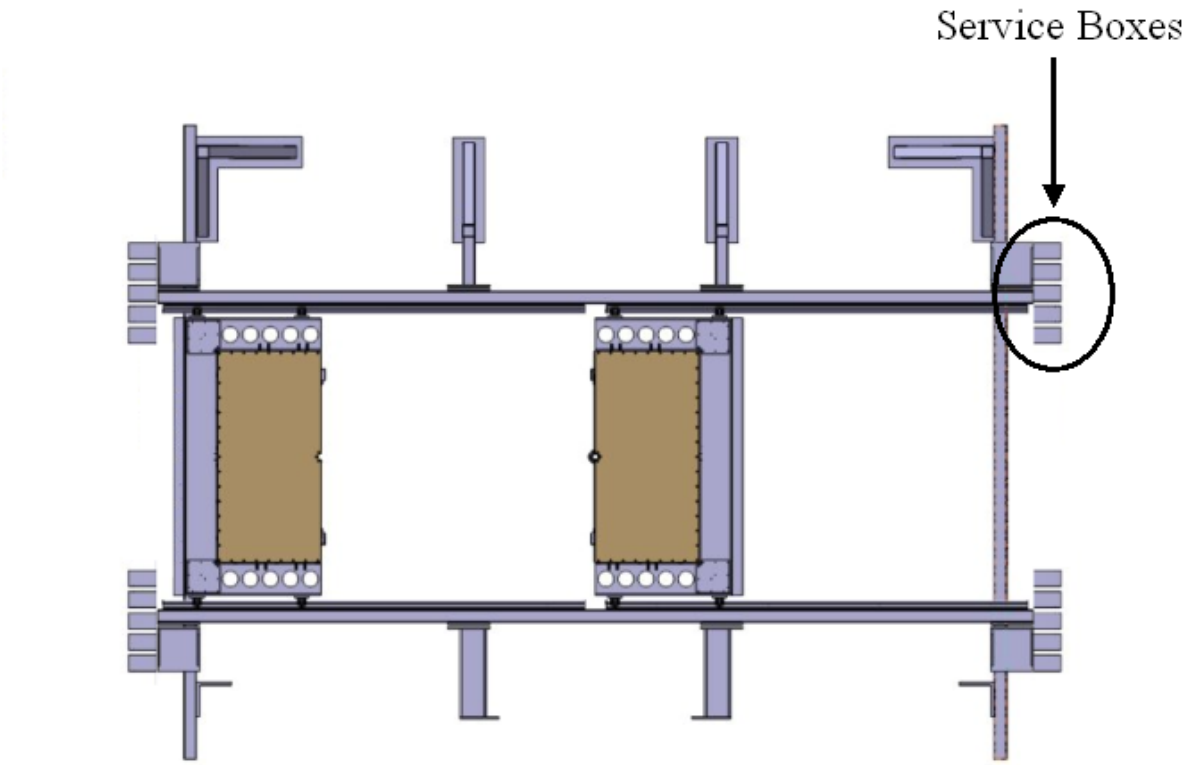

Figure 10.29: Proposed location for the Trigger Tracker Service Boxes at the TT station support frame (left side of the station opened).

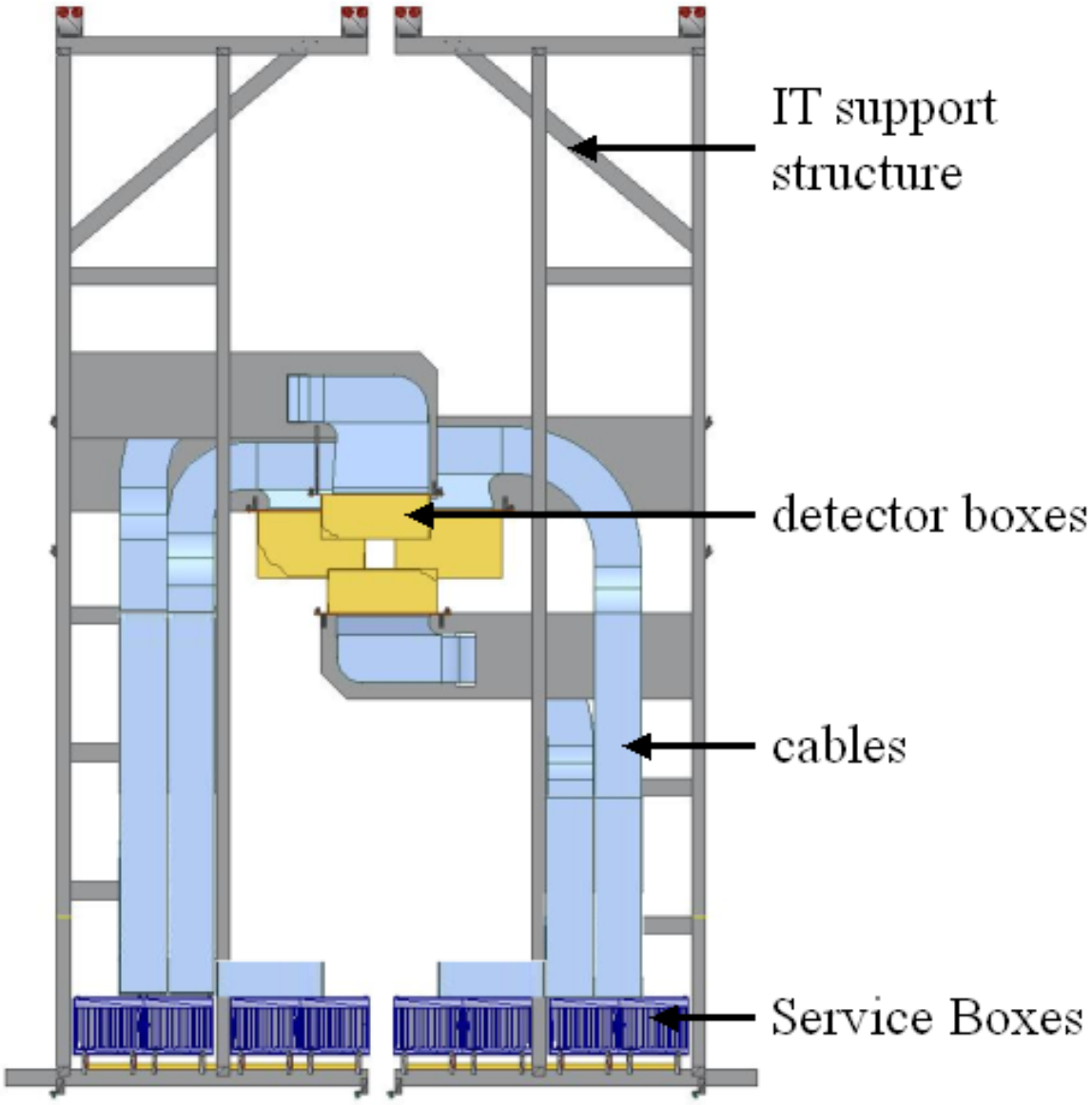

Figure 10.30: Proposed location for the Inner Tracker Service Boxes at the bottom of the IT station support frame (only one tracking station shown).

Chapter 11

Connection to LHCb DAQ

The next level of data processing occurs after the transmission of the data from the detector to the counting house. As a part of the Silicon Tracker data is used for the Level-1 trigger decision, the data is processed twice in parallel: once for the Level-1 trigger and once for later analysis by the higher level trigger (HLT). This processing is performed on custom-designed boards, the so-called TELL1 boards [63]. They are equipped with optical receiver cards (O-RX-cards) for direct connection to the optical fibres coming from the detector.

11.1 The Optical Receiver Card (O-RX-card)

The development of the optical receiver card (O-RX-card) is led by the Outer Tracker group at the University Heidelberg [62]. As it became clear early on the design of the optical readout link, that the OT and the ST will share major elements of the readout system, it was decided to follow a common path which led to the development of the O-RX-card.

The O-RX-card is based on using a parallel optical receiver in conjunction with 12 de-serializers, which are compatible with the GOL encoded format provided by the on-detector electronics. To maintain as much flexibility as possible, a generic socket compatible with the SNAP12 industry standard for parallel optical modules was chosen as a receptacle for the receiver. By adding some optional solder contacts, the design became compatible to a number of receiver devices, which are available on the market and share the same optical and electrical interfaces. One advantage of this approach is that the board does not depend on a single supplier for optical modules, but leaves the user with the possibility to change to different devices, when needed. This proved to be very helpful as during the prototyping stage some of the companies withdrew their product from the market while others even expanded their portfolio. Another advantage is that it is possible to have the whole O-RX-card populated and reflow soldered without the optical receiver but only the SNAP12 socket. This eliminates the risk of thermally damaging the optical module during the solder process.

For the Silicon Tracker, the MRX-9512 produced by Emcore Corp. was chosen (see Figure 11.2). The output of the receiver is connected to 12 TLK2501 Gigabit deserializers produced

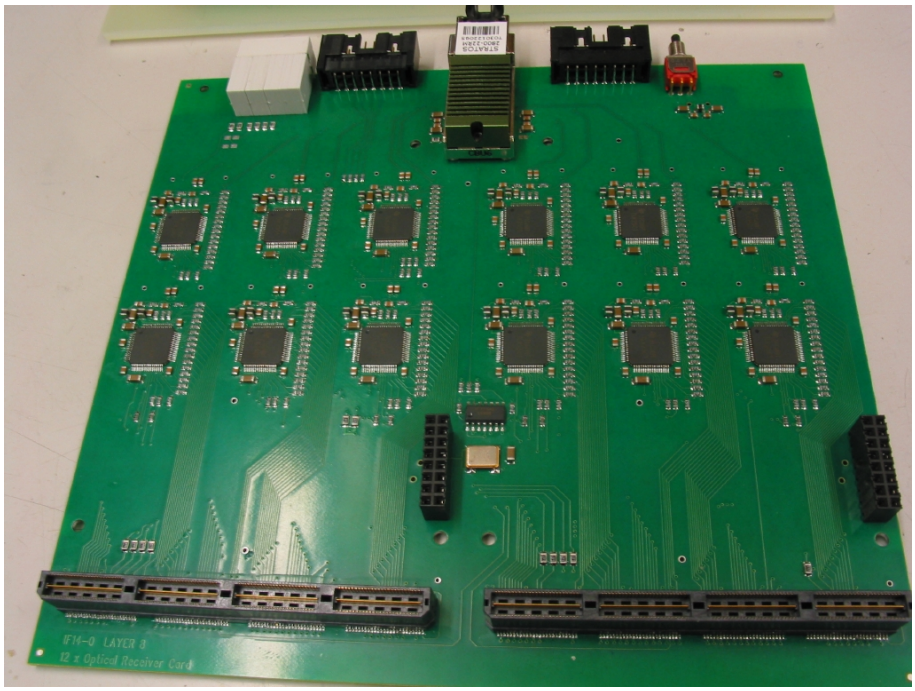

Figure 11.1: The O-RX-Card, developed by the OT group, University Heidelberg.

by Texas Instruments [27]. Only the deserializer part of the device is used, although it is equipped with a serializer and a deserializer for full duplex operation. A custom-cut, low-jitter crystal oscillator with double the LHC clock frequency is used to provide the on-chip PLL[1] with a reference frequency to enable the clock recovery circuit to lock to the incoming data stream. A stand-alone oscillator is sufficient for the operation of the TLK2501, as long as the initial frequency is within 100 ppm of the clock frequency of the incoming data stream. The exact phase lock is then established by the PLL circuit of the TLK2501 itself. No other input aside from the optical input signals and the power supply is needed.

The TLK2501 performs a 1:16 deserializing at twice the LHC clock frequency, while the GOL performs a 32:1 serializing at LHC clock frequency. The additional 1:2 demultiplexing to obtain the original format of 32 bits is performed in the first stages of the TELL1 board (see Section 11.2).

The overall power consumption is dominated by the 12 deserializers, which are dissipating 260 mW when running at 1.6 Gbit/s. With a power dissipation of the optical receiver of approximately 1.2 W, the total power dissipation of each O-RX-card is close to 4.5 W.

[1]PLL: phase-locked loop

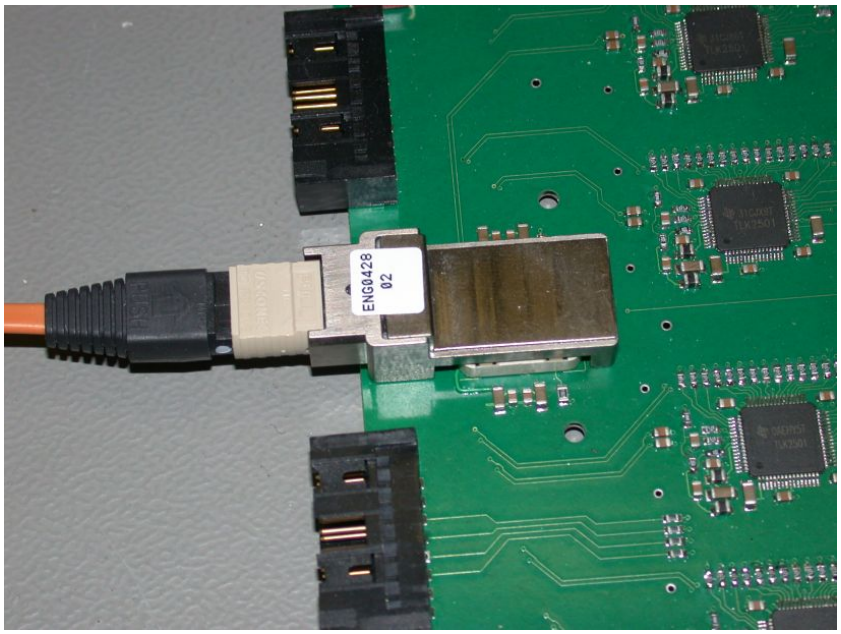

Figure 11.2: A SNAP12 compatible optical receiver on the O-RX card.

11.2 The TELL1 Board

The Trigger ELectronic and Level-1 (TELL1) board was developed at the EPF Lausanne in an effort to unify the preprocessing boards for the various LHCb subdetectors. The adaption to the requirements of different detectors and readout schemes is possible by using reprogrammable FPGA devices as baseline technology. A picture of a prototype board is shown in Figure 11.3. As of 2004, the Vertex Locator with the Pile-Up detector, the Silicon Tracker, the Outer Tracker, the Calorimeter and the Muon detector are going to make use of the TELL1 board.

The main functionality of the TELL1 board is implemented in four preprocessing FPGAs (PP-FPGAs), which perform initial processing on the incoming digital data. The data may enter the TELL1 board via the O-RX card (see Section 11.1) as in the case of the Outer Tracker or Silicon Tracker, or via ADC cards, as in the case of the Vertex Locator. First, in the Silicon Tracker PP-FPGAs, the 32 original bits of the GOL encoding are restored. In addition, the received pipeline column number can be compared to a frontend emulator on the TELL1 board for synchronicity checks. In the next step, a two-loop linear common mode rejection algorithm is applied to subtract the noise contribution that is common to all channels on a Beetle readout frame. Signals, which exceed a given noise level are then detected as hits and stored for further analysis. As hits in the Trigger Tracker are used for the Level-1 trigger decision, the TELL1 boards have a two-fold datapath integrated, with one path generating data for the Level-1 algorithm and a second path doing a refined hit finding analysis for use in the HLT. The data from all 4 PP-FPGAs is linked together in the

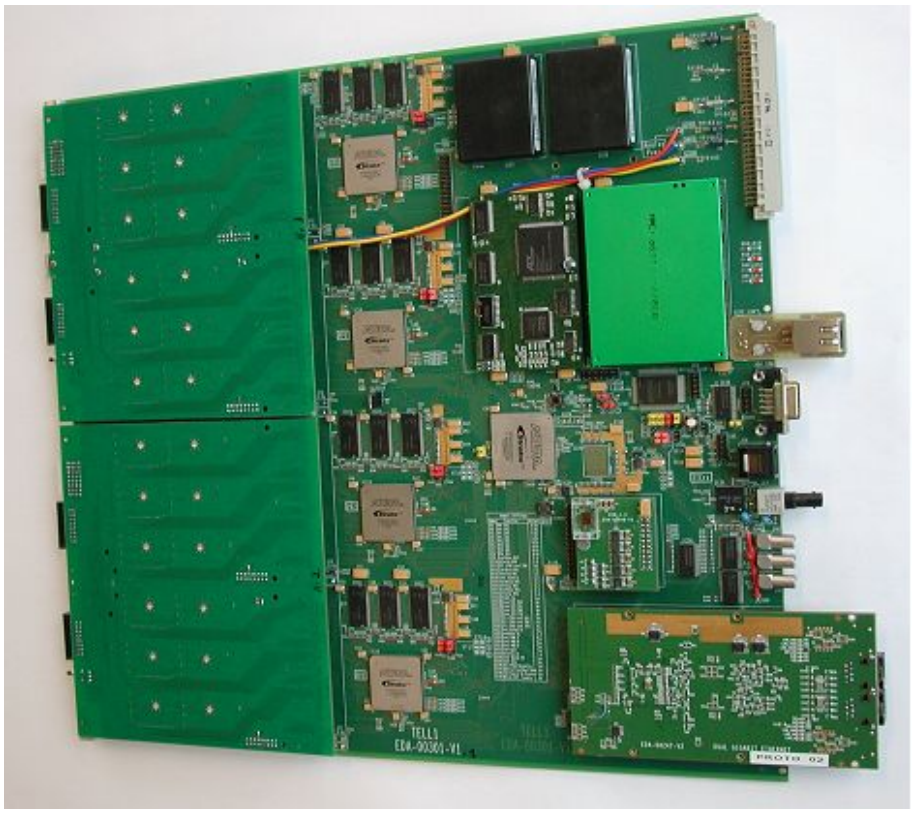

Figure 11.3: The TELL1 board, developed by G. Haefeli/EPF Lausanne.

SyncLink-FPGA, which packs the data into TCP/IP frames for transmission over the TELL1 Gigabit Ethernet interface to the Readout Network. More information about the TELL1 board can be found in [63] and [64].

11.3 DAQ Partitioning

The DAQ partitioning describes the association between readout hybrids and TELL1 boards. The key requirements here are the limited Level-1 data rate capability for a single TELL1 board and the goal to preserve the highest possible track finding efficiency in case of a single component failure.

For the Trigger Tracker, six frontend hybrids (equivalent to six readout sectors) are read out with one TELL1 board. Figures 11.4 and 11.5 shows the proposed partitioning, which for a total of 280 readout sectors requires 48 TELL1 boards

Each TELL1 board only serves readout sectors within a single detection layer. By doing so, not only an easier mapping is provided but also a larger tolerance to single component failures is achieved. A failure of one TELL1 board will result in missing hit information from one detection layer, but track finding, with slightly reduced efficiency and precision, is

still possible using hits from the other three layers of the station. In a partitioning where a single TELL1 board serves 4 detection layers arranged just behind each other, a board failure would leave the Trigger Tracker with a sizeable area in the acceptance area of the experiment without any track information at all.

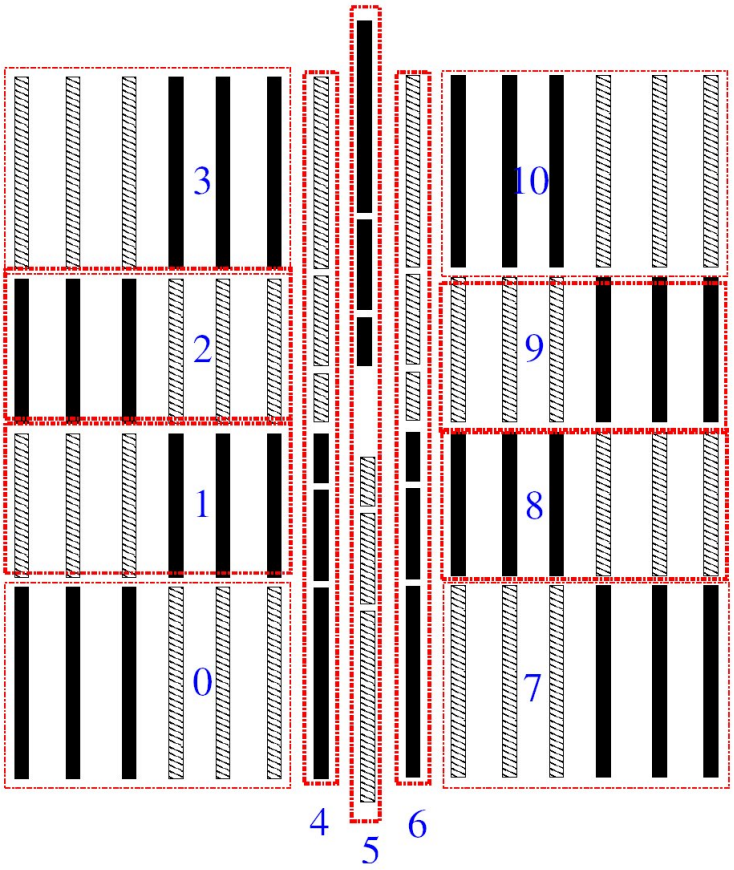

Figure 11.4: Partitioning for one layer of the TTa station.

The grouping with dashed lines and the numbers represent different TELL1 boards, while the pattern of the readout modules within a TELL1 group represents the associated optical fibre ribbon (each TELL1 board receives data from two fibre ribbons).

For the Inner Tracker,each hybrid carries only three Beetle readout chips. Each Inner Tracker TELL1 board can therefore handle up to eight readout hybrids, which is equivalent to eight sensor ladders. As each detector box holds 28 sensor ladders, four TELL1 boards would be needed per detector box, of which the fourth board would only be used half. However, one TELL1 board can accept data from two different detector boxes to save on the number of TELL1 boards. Similar to the partitioning in the Trigger Tracker, no TELL1 board processes data from all four detection layers of a station to prevent a single failure leading to a complete loss of hit information. The proposed layout is shown in Figure 11.6.

For a more in-depth discussion on the data format for raw data and Level-1 data and the associated load on the TELL1 boards, see [61].

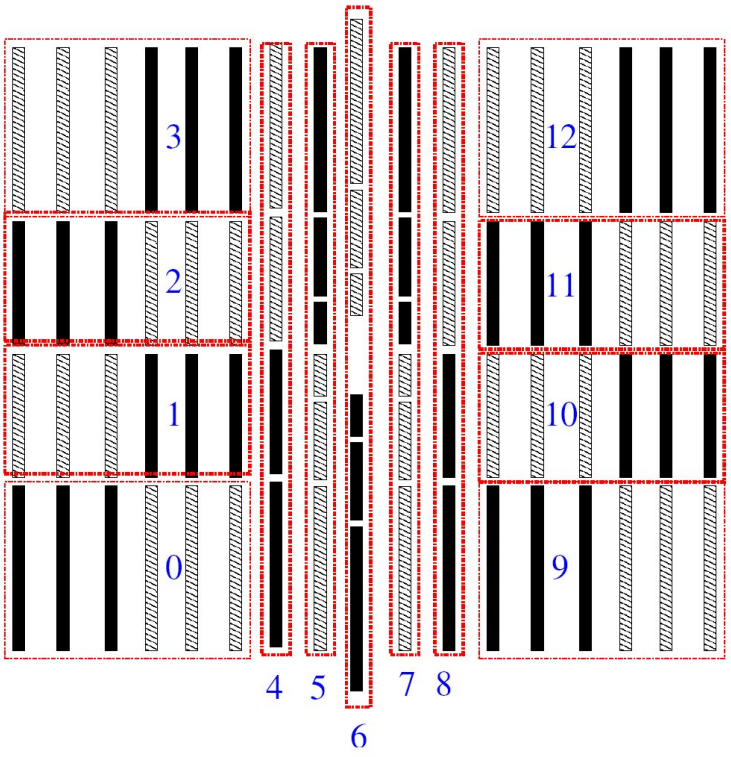

Figure 11.5: Partitioning of one layer of the TTb station.

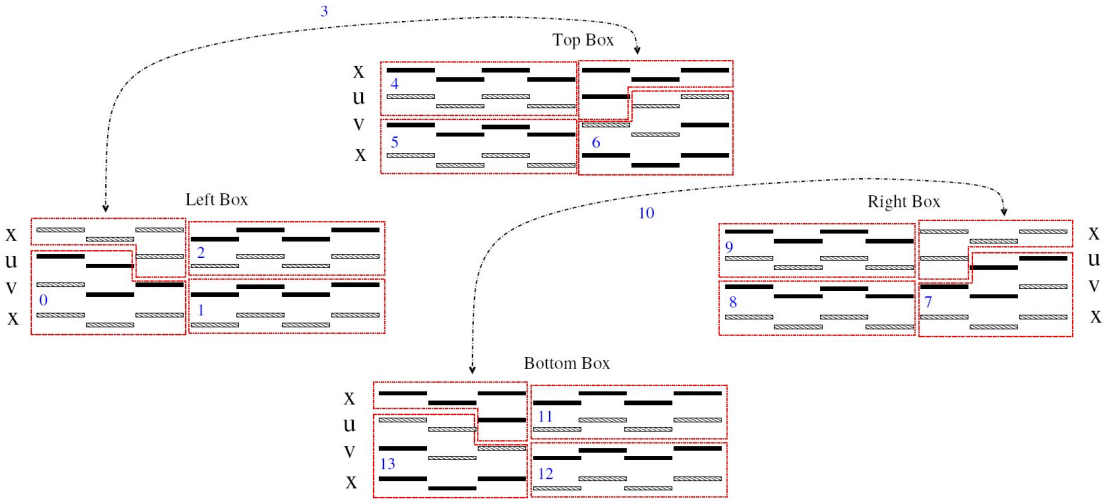

Figure 11.6: Partitioning of one detector box of the IT detector.

Chapter 12

Common LHCb Optical link

In meetings and discussions with other LHCb subdetector groups, while prototyping the Silicon Tracker readout link, it became clear that the groups had similar readout requirements. The Muon Trigger group had also started R&D for a very similar readout system and the Outer Tracker group was developing a digital optical link as well. An effort for a common LHCb optical link was thus initiated in 2003, trailing the already started unification of the Level-1 preprocessing boards into the TELL1 board. Together with the O-RX card, which was originally planned for use in the Silicon Tracker and Outer Tracker only, the TELL1 board provides a flexible and robust interface for connection to the DAQ network. The combination of the GOL serializer together with the VCSEL diode has been adapted by several other detectors, although solutions using parallel optical transmitters instead of the single VCSEL diodes are favored in areas without radiation. Common for all users of the digital optical link is the multi-channel ribbon fibre with a core size of 50 μm.

Further common efforts concern the coordination of the cable installation and the selection of optical patch panels. The patch panels not only provide the possibility to exchange irradiated ribbon cable sections, but also define the logistical interface between the area of responsibility of the CERN group, which is responsible for the installation of the long fibre section from the cavern to the counting house, and that of the subdetector groups, which have to connect locally their subdetectors to the patch panel in the cavern and the according fibre cables to the TELL1 boards in the counting room.

The benefits of this joint effort are increased order volumes and reduced prices for components like optical fibre, VCSEL diodes, transmitter and receiver modules and commercial deserializers. Furthermore, the workload during R&D phase, commissioning, operation and maintenance for individual groups was significantly reduced.

Conclusion

The LHCb Silicon Tracker provides tracking information for the high track density regions of the LHCb experiment. The Silicon Tracker is divided into a Trigger Tracker upstream of the spectrometer magnet and an Inner Tracker downstream of the magnet. The principle of using silicon strip detectors together with radiation-hard multi-channel charge integrating amplifiers is common for both subsystems. A common data transmission system, which is the scope of this work, has been developed to transport the 2.7 Terabit/s detector data rate over a distance of 100 m from the detector to the counting house.

Having identified the requirements of the Silicon Tracker and evaluated the possible transmission systems, it was decided to develop a digital optical transmission system. This solution features numerous advantages, such as greatly reduced immunity to external electromagnetic interference, a galvanic isolation between transmitter and receiver and reduced cross section of the cables that are used for data transmission. The expected performance was verified with prototype circuits in the development phase.

As the transmitting part of this readout system is located close to the detector, it will be exposed to ionizing radiation.Radiation qualification was needed for active devices and optical components. Appropriate environments for irradiation tests were chosen according to the technology of the components and test setups were developed to determine cummulative and single event effects. Irradiation with neutrons and protons with doses corresponding to multiples of those expected for a 10-year operation of the experiment were performed. All devices under test were determined to be sufficiently radiation tolerant for their proposed location.

The interfaces to the LHCb Timing and Fast Control network as well as to the LHCb Experiment Control System have been defined. The Service Box, as the key element of the development described in this work, houses all necessary on-detector electronics apart from the detector readout hybrid. The analogue data coming from the Beetle readout amplifiers is received by the Digitizer Boards, which digitize 12 or 16 channels, depending on their assignment to either the Inner Tracker or the Trigger Tracker. The digitized data is encoded with the GOL serializer and transmitted via single VCSEL diodes into multimode optical fibre. The initial single fibres are subsequently grouped into 12-channel ribbon cable and into 8-ribbon cable tubes, which provide denser packing factors and enhanced mechanical robustness. Further elements of the Service Box are the backplane, which provides regulation of the supply voltages and distribution of the signals to the Digitizer Boards, and a Control Card serves as the interface to the TFC and ECS systems.

In the counting house, the data is received by multi-channel optical receivers located on the O-RX cards, which are mounted on the TELL1 board. On the TELL1 board, the data is preprocessed for transmission into the Level-1 trigger and the DAQ network.

All LHCb subdetectors using optical transmission systems are building a common LHCb optical link, which uses many of the components described in this work.

The next steps include the start of the series production for the Silicon Tracker to be ready for installation into the LHCb detector in 2006. After successful commissioning, the first data-taking of LHCb is expected for late 2007.

Appendix A

Pin Assignments

Table A.1: Pin assignment of the Digitizer Board's front connector (X1).

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	*AnaOut0*	35	*notAnaOut0*	18	*AnaOut14*	52	*notAnaOut14*
2	*AnaOut1*	36	*notAnaOut1*	19	*AnaOut15*	53	*notAnaOut15*
3	*AnaOut2*	37	*notAnaOut2*	20	*Beetle_GND*	54	*Beetle_GND*
4	*AnaOut3*	38	*notAnaOut3*	21	*VDD_SENSR*	55	*VDD_SENS*
5	*AnaOut4*	39	*notAnaOut4*	22	*VDDD_SENSR*	56	*VDDD_SENS*
6	*AnaOut5*	40	*notAnaOut5*	23	PT4	57	PT6
7	*Beetle_GND*	41	*Beetle_VDD*	24	*I2C_ADR5*	58	*I2C_ADR6*
8	*Beetle_GND*	42	*Beetle_VDD*	25	*Beetle_DGND*	59	*Beetle_VDDD*
9	*Beetle_GND*	43	*Beetle_VDD*	26	*Beetle_DGND*	60	*Beetle_VDDD*
10	*AnaOut6*	44	*notAnaOut6*	27	*Beetle_DGND*	61	*Beetle_VDDD*
11	*AnaOut7*	45	*notAnaOut7*	28	*Beetle_DGND*	62	*Beetle_SCL*
12	*AnaOut8*	46	*notAnaOut8*	29	*Beetle_DGND*	63	*Beetle_SDA*
13	*AnaOut9*	47	*notAnaOut9*	30	*noDataValid*	64	*DataValid*
14	*AnaOut10*	48	*notAnaOut10*	31	*notTESTPULSE*	65	*TESTPULSE*
15	*AnaOut11*	49	*notAnaOut11*	32	*notTRIGGER*	66	*TRIGGER*
16	*AnaOut12*	50	*notAnaOut12*	33	*notRESET_BEETLE*	67	*RESET_BEETLE*
17	*AnaOut13*	51	*notAnaOut13*	34	*notCLK_BEETLE*	68	*CLK_BEETLE*

Type of connector: VHDCI, Honda HDRA-EC68-LFDT-SL

Remark to Table A.1: For an IT Digitizer Board, Pins 16-19 and 50-53 are identical to *Beetle_GND*, as a IT Digitizer Board only reads out a 3-chip Beetle hybrid.

Table A.2: Pin assignment of the Digitizer Board's rear connector (X2).

Pin	Signal	Pin	Signal	Pin	Signal
A1	*OCM_ANA*	B1	*Beetle_GND*	C1	*CLK_ADCGOL*
A2	*OCM_DIG*	B2	*Beetle_GND*	C2	*notCLK_ADCGOL*
A3	*Beetle_VDDD*	B3	*Beetle_GND*	C3	*CLK_BEETLE*
A4	*Beetle_VDDD*	B4	*VDD_SENSR*	C4	*notCLK_BEETLE*
A5	*Beetle_VDDD*	B5	*Beetle_DGND*	C5	*RESET_BEETLE*
A6	*VDDD_SENS*	B6	*Beetle_DGND*	C6	*notRESET_BEETLE*
A7	*Beetle_VDD*	B7	*Beetle_DGND*	C7	*TRIGGER*
A8	*Beetle_VDD*	B8	*VDDD_SENSR*	C8	*notTRIGGER*
A9	*Beetle_VDD*	B9	*GND*	C9	*TESTPULSE*
A10	*VDD_SENS*	B10	*GND*	C10	*notTESTPULSE*
A11	*+5 V*	B11	*GND*	C11	*BeetleSDA*
A12	*+5 V*	B12	*GND*	C12	*BeetleSCL*
A13	*VDD*	B13	*GND*	C13	*DCUGOLSDA*
A14	*VDD*	B14	*QPLL_RESET*	C14	*DCUGOLSCL*
A15	*VDD*	B15	*GOL_RESET*	C15	*I2C_ADR5*
A16	*VDD*	B16	*notGOL_RESET*	C16	*I2C_ADR6*

Type of connector: DIN41612 version C, 3 rows with 16 pins male, angled

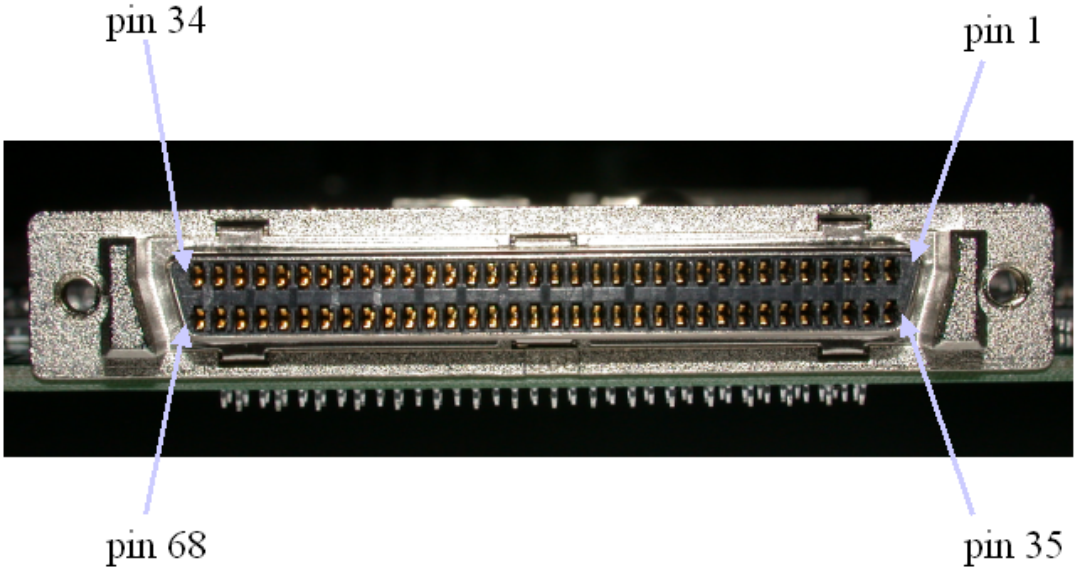

Figure A.1: View of the front connector X1.

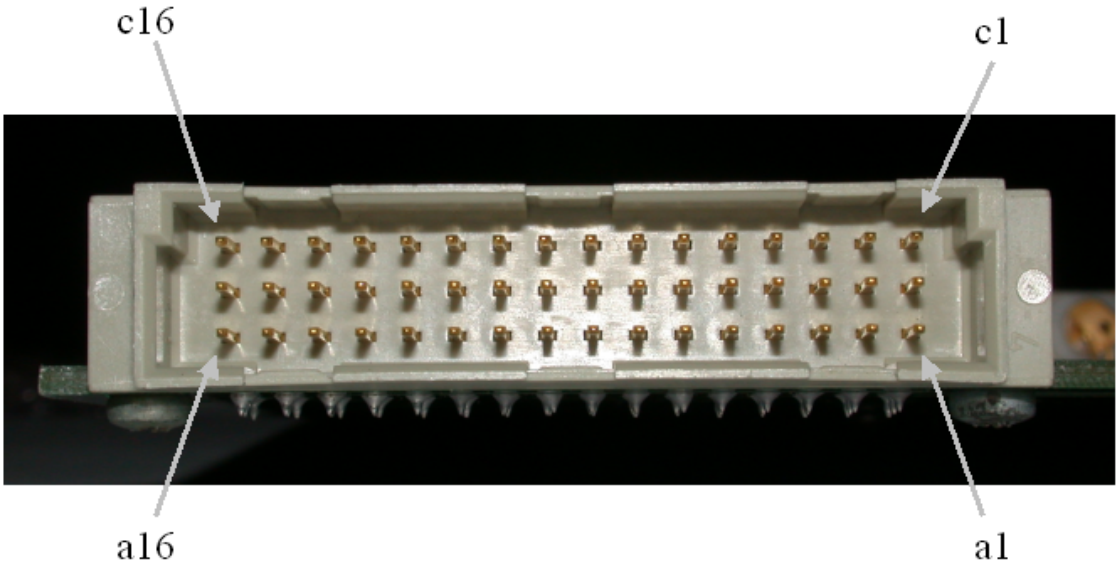

Figure A.2: View of the rear connector X2.

Appendix B

Digitizer Board Schematic Diagrams

The schematic diagrams showed here are only displaying single instances of recurring building blocks due to space limitations. For a complete schematic diagram and layout data, refer to the CERN EDMS database.

In addition, the bugs and errors which were found during characterization of the Digitizer Board are listed. All of those will be corrected for the final version of the boards.

- Figure B.1: connect REF pin of AD8129 to VDD instead to reference voltage of ADC.
- Figure B.1: lower impedance of R119/R120 divider from 1 kΩ:1 kΩ to 270 Ω:330 Ω.
- Figure B.2: Pinout of the VCSEL diode wrong.
- Figure B.3: add missing termination to incoming CLK_ADCGOL line at IC6.
- Figure B.4: include RC-network at node X1 of QPLL to reduce crystal drive (as proposed by P. Moreira in Nov. 2004).
- Figure B.4: swap default phase of GOLCLK by populating R28/R30 instead of R27/R29.
- Figure B.5: swap default clock phase for ex64 by populating R41 instead of R42.
- Figure B.6: connect REF pin of AD8129 to VDD instead to GND.

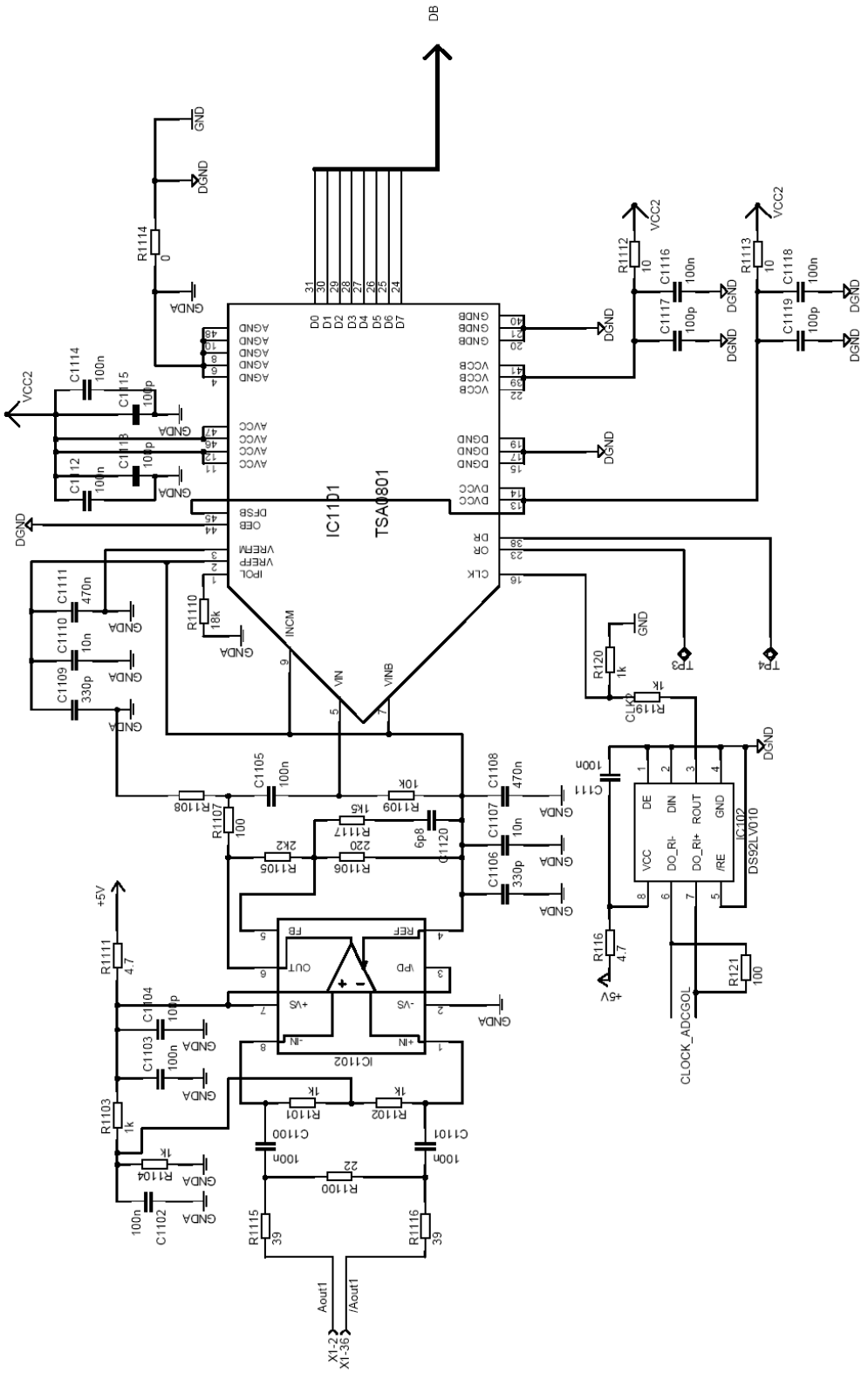

Figure B.1: Schematic diagram of the line receiver stage for channel 1 with ADC.

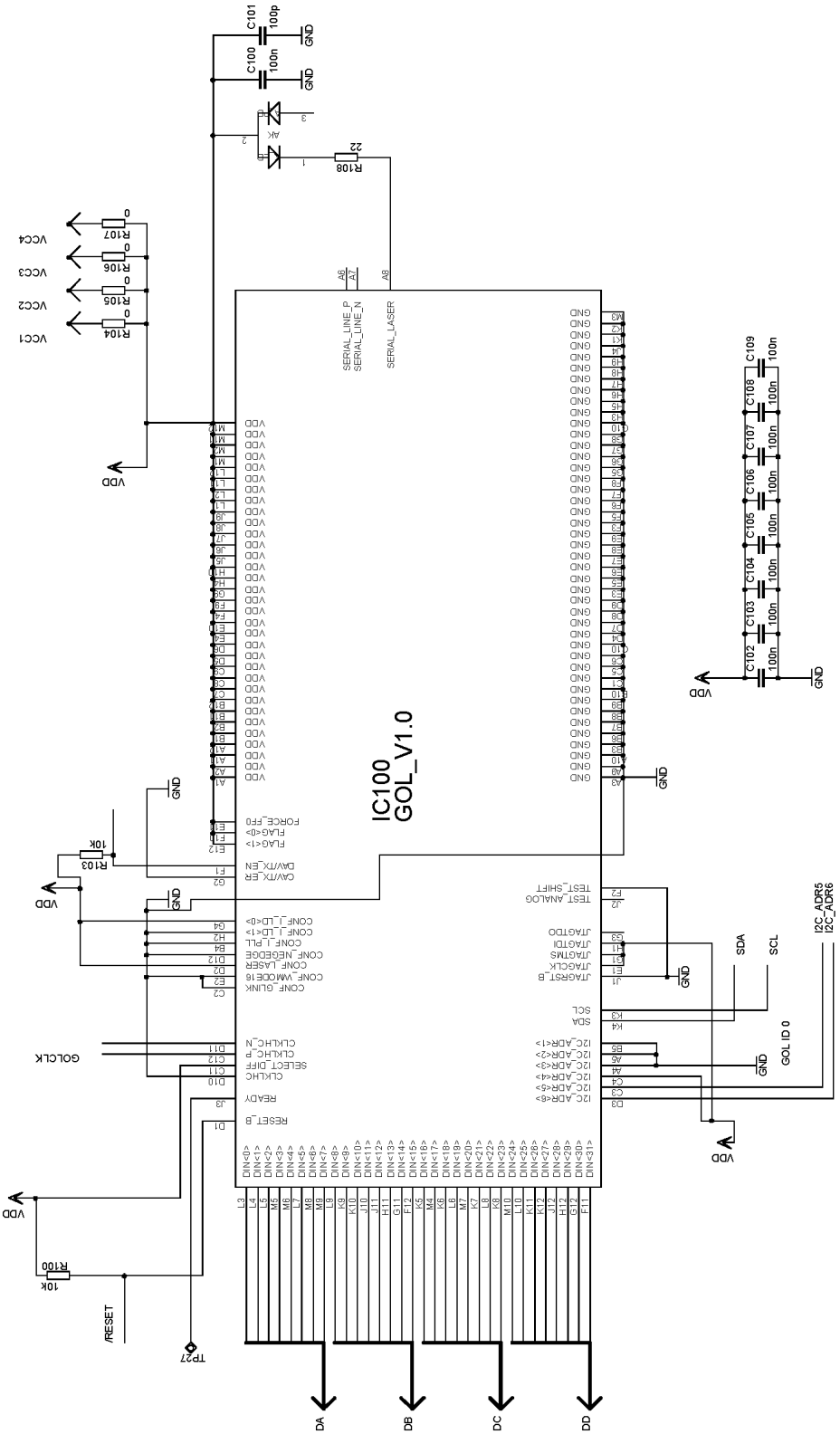

Figure B.2: Schematic diagram of the GOL serializer for channels 0-3.

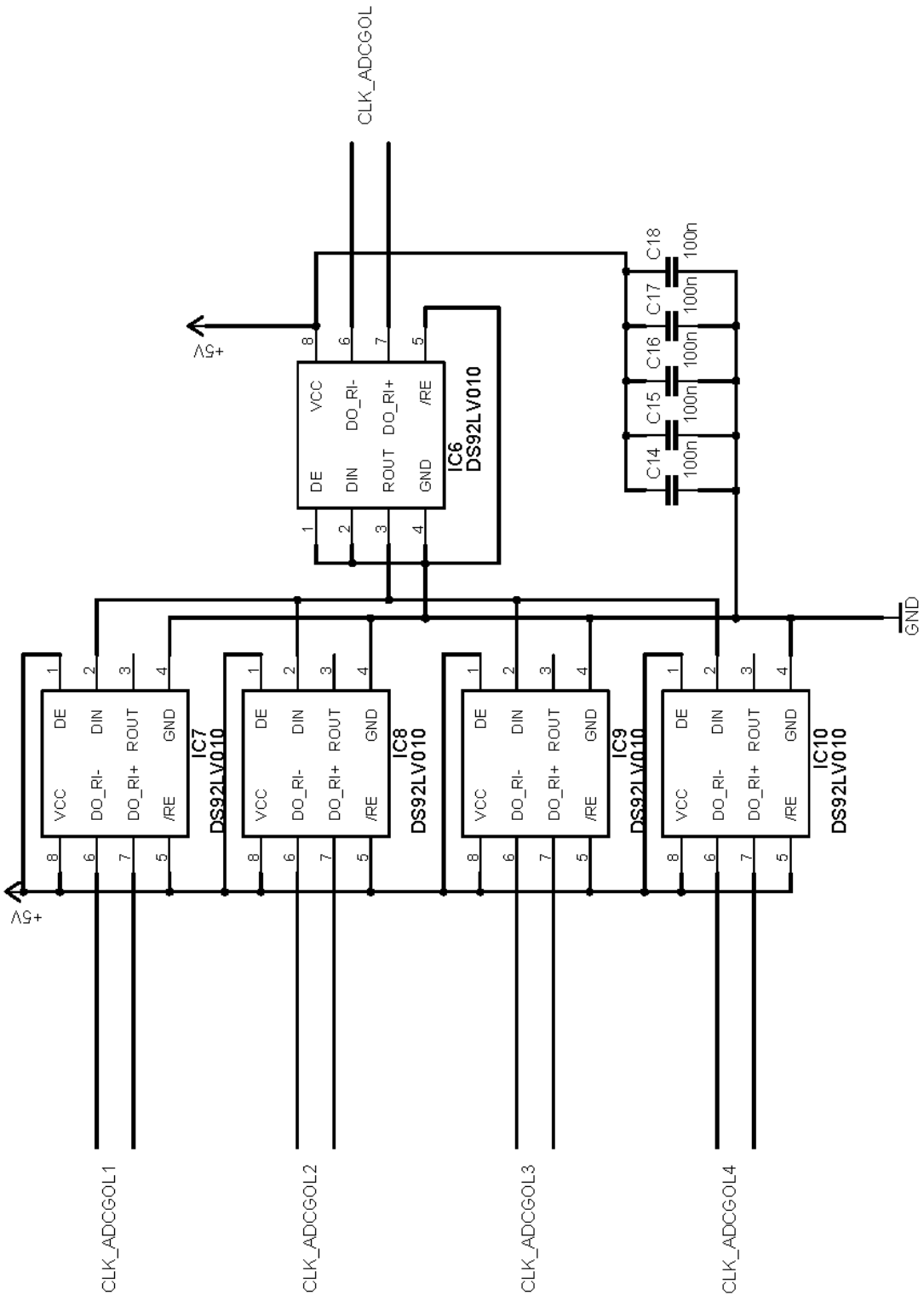

Figure B.3: Schematic diagram of the clock distribution for the ADCs.

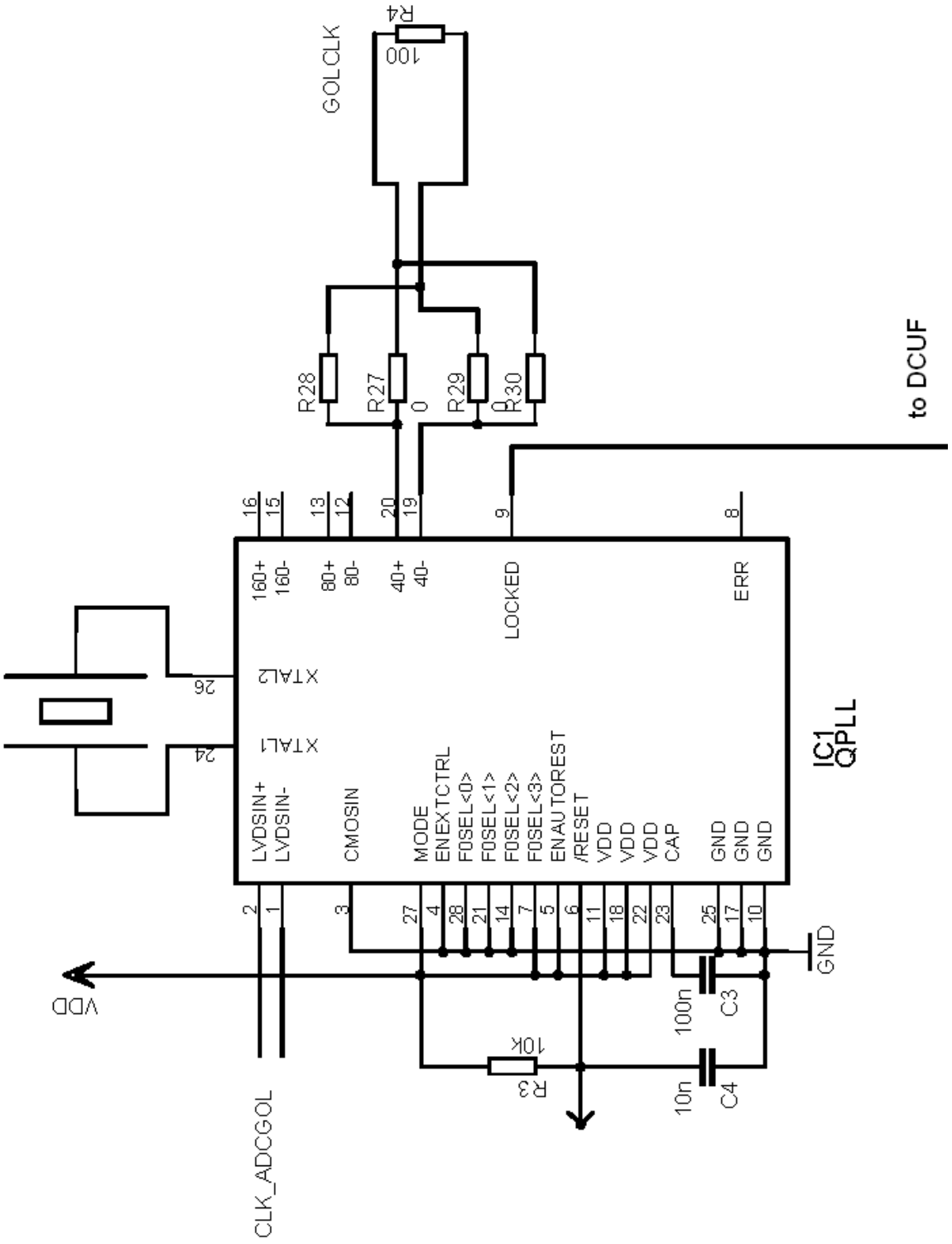

Figure B.4: Schematic diagram of the QPLL clock circuit.

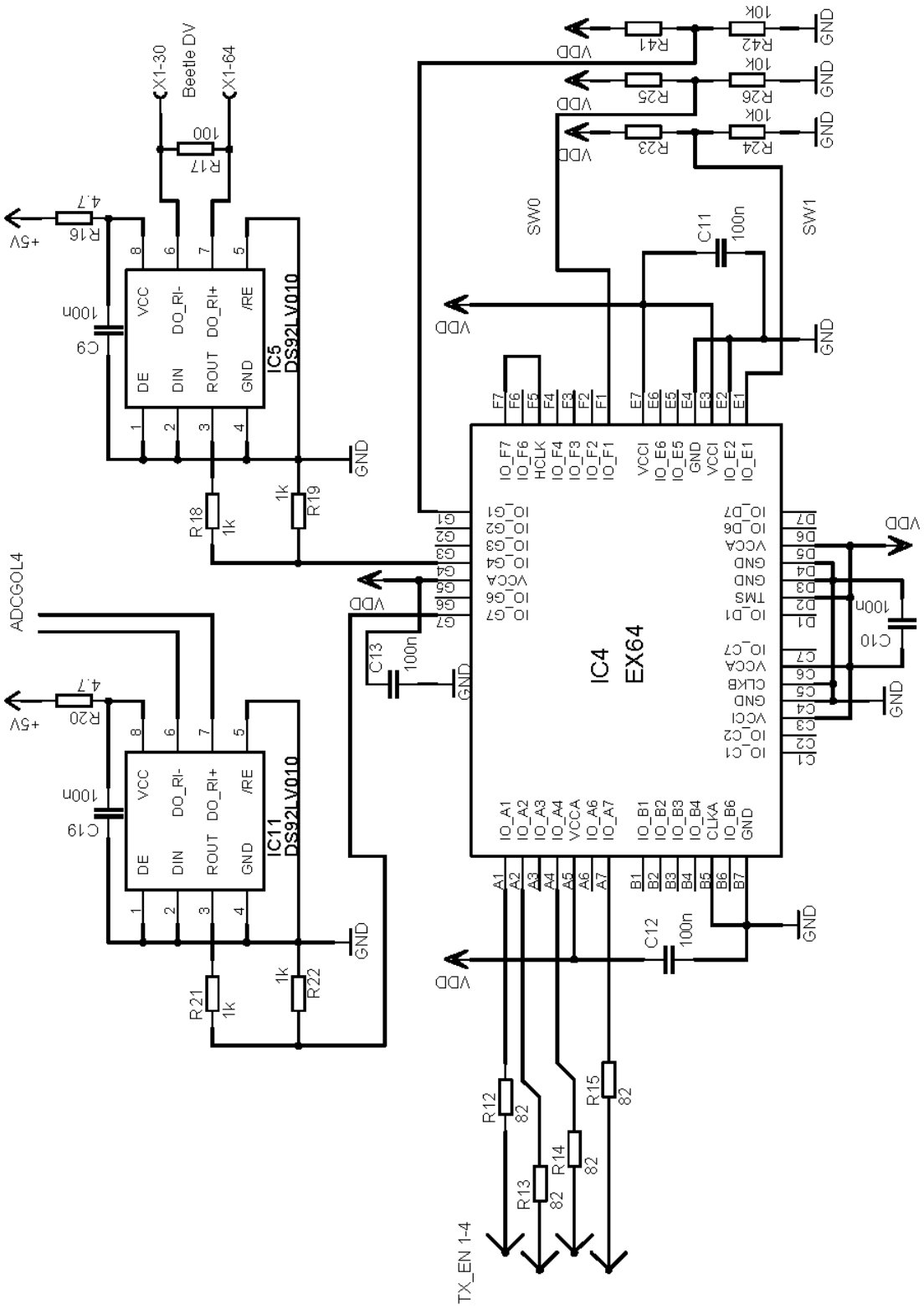

Figure B.5: Schematic diagram of the synchronization shift-register.

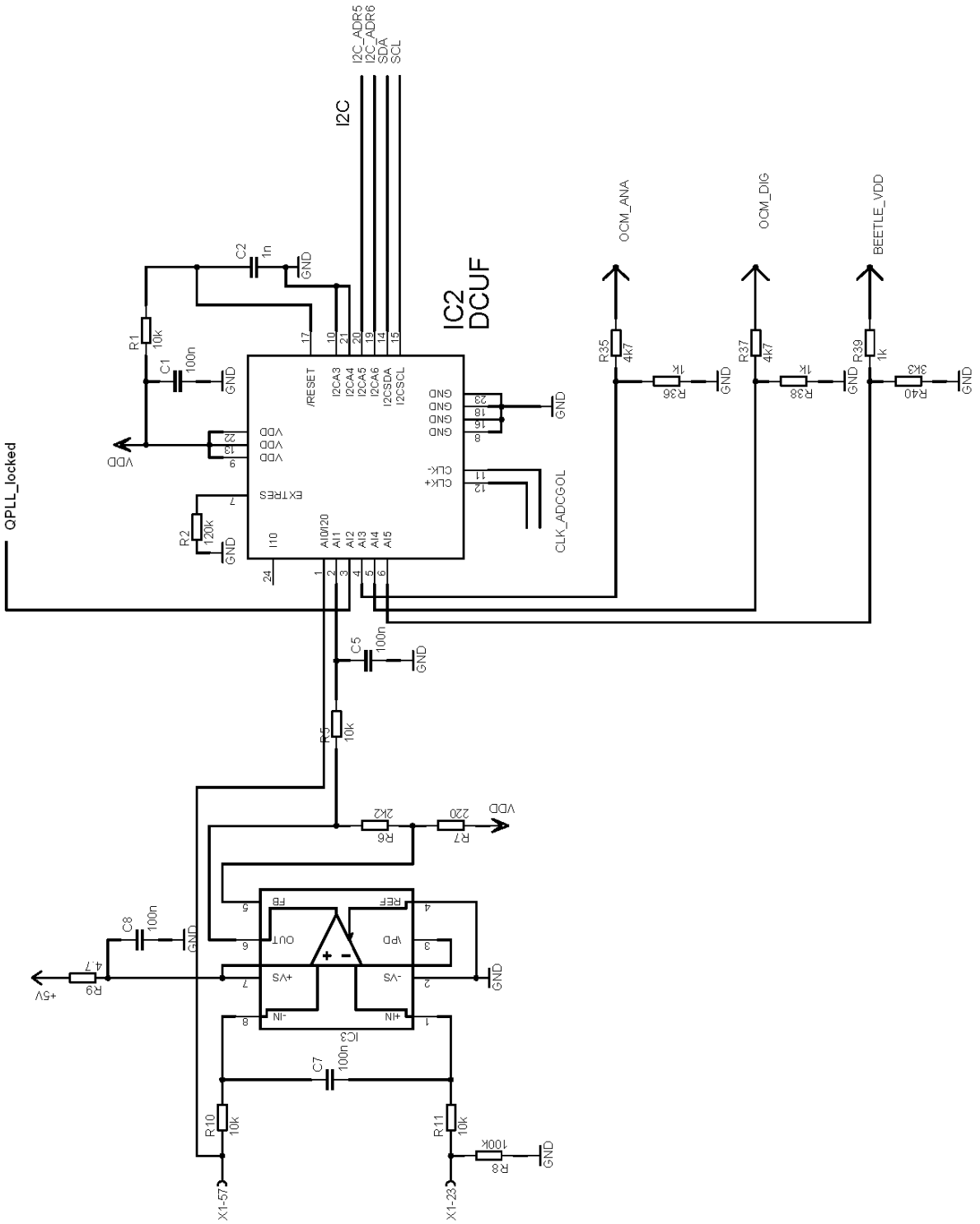

Figure B.6: Schematic diagram of the DCUF slow control ADC.

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